Chapter 14

- Dynamic Logic Gates
  - Fundamentals
  - Simulations
  - Non-Overlapping Clock
  - CMOS TG in Dynamic Circuits
  - Clocked CMOS Logic
    - Clocked Latch
    - Pre-charge Evaluate (PE) Logic
    - Domino Logic
    - NP (Zipper) Logic
  - Dynamic Latch, Register
DYNAMIC CIRCUITS

FUNDAMENTALS

- CAPACITANCE STORES CHARGE
  - “DYNAMIC” LOGIC
  - SUSCEPTIBLE TO NOISE
- PG=H
  - IN=VDD, NODE B→VDD-Vtn
  - IN=GND, NODE B→GND
- PG=L
  - NODE B=VDD-Vtn → GND
  - NODE B=GND
- TIME THAT CHARGE REMAINS?

- OFF-STATE CURRENT
  - S/D TO BODY LEAKAGE
  - POLY TO FOX EDGE LEAKAGE
  - SOURCE TO DRAIN LEAKAGE
- LOG(Id)=-8.45
- Id = 10^{-8.45} = 3.55nA
- Ioff ~ 7.1nA / um → GOOD METRIC
- \( \frac{dV}{dt} = I_{off} \times \frac{W}{C_{node}} \)

Figure 14.1 Example of a dynamic circuit and associated storage capacitance.

Figure 14.2 Drain current of an NMOS device plotted from weak to strong inversion. See Fig. 6.16. PMOS netlist is found at cmoseedu.com.
**DYNAMIC CIRCUITS**

- 10/1
- Initially charge to 1 V
- 50 fF

**FUNDAMENTALS**

- **EXAMPLE 14.1**
  - \( \frac{dV}{dt} = \frac{3.55 \text{nA}}{50 \text{fF}} = 71 \text{mV/\mu s} \)
  - IF INITIAL CHARGE=1V,
    \( t = \frac{1 \text{V}}{(0.071 \text{V/\mu s})} = 14 \text{us} \)
  - SIMULATION RESULTS, \( t=30 \text{us} \)
  - WHY IS IT DIFFERENT?
    - WHAT IS SOURCE-BULK VOLTAGE?

- **EXAMPLE 14.2**
  - KEEP INPUT AT VDD/2, NOT GND
  - VDS NOW LOWER

**Figure 14.4** Time it takes the capacitor to discharge due to the off current of the MOSFET in Fig. 14.3.

**Figure 6.19** Current-voltage characteristics for 50 nm MOSFETs.
**LOGIC – DYNAMIC CMOS**

- Non-overlapping (NOL) clock
  - Needed for 2-phase clock systems
  - Similar to master-slave FF
  - Clocks out of phase
  - Matching in routing, xors

**EXAMPLE CIRCUITS**

- **Dynamic Shift Register**
  - NOL clock
  - A0 – A3 data lines
  - Shifts through with clock

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Figure 14.9 Nonoverlapping clock generation circuit.

Figure 14.8 Dynamic shift register with associated nonoverlapping clock signals.
LOGIC – DYNAMIC CMOS

DESCRIPTION

DIFFERING DEFINITIONS
- CLOCKED IN SOME SECTIONS
- PARASITICS AS PART OF CIRCUIT

PROS
- ONE TRANSISTOR, VERY SMALL
- FAST

CONS
- DATA TRANSIENT
- SUBJECT TO NOISE
- PTV DELTAS
  - PROCESS, TEMP, VOLT

OPERATION
- CONTROL GATE PULSED HIGH
- INPUT A TRANSFERRED TO B
- CONTROL GATE GOES LOW
- NODE B CONTAINS VDD-Vtn
- REFRESH DATA OR OUTPUT CHG

SIMULATIONS
- GMIN IS A SHUNT RESISTOR ACROSS DIODES
- USE DEFAULTS, BUT KEEP IN MIND
- dV/dt~200uV/us

Figure 14.10 CMOS TG used in dynamic logic.
Baker Ch. 14 Dynamic Logic Gates

Introduction to VLSI

LOGIC – CLOCKED CMOS

DESCRIPTION
- CLOCK USED TO ACTIVATE GATE
- SIMILAR TO TRI-STATE INVERTER
- PROS
  - BETTER ISOLATION
  - NO RACE CONDITIONS
  - REDUCED XTOR COUNT VS. CMOS
- CONS
  - MORE COMPLICATED
  - NEED 2-PHASE CLOCK

CLOCKED INVERTER

Figure 14.11 A clocked CMOS latch. The clock signals can be generated with an RS latch so that the edges occur essentially at the same moment in time.
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**LOGIC – PE**

**PRE-CHARGE EVALUATE (PE)**

- **OPERATION**
  - OUTPUT PRE-CHARGED BY PMOS
  - CLK ACTIVATES NMOS SECTION
  - CLK=L, N-OFF, P-ON, OUT-H
  - CLK=H, N-ON, P-OFF, OUT-LOGIC

- **PROS**
  - OUTPUT CAP LOWER
  - SINGLE GATE PER INPUT
  - LOWER POWER DISSIPATION
  - FASTER

- **CONS**
  - OUTPUT LOGIC ONLY VALID WHEN CLOCK IS HIGH VS. STATIC LOGIC
  - GLITCH IN TIME BETWEEN PRE-CHARGE AND EVALUATE CASCADES DOWN CHAIN
  - DOMINO LOGIC SOLVES PROBLEM
LOGIC – DOMINO, NP

DESCRIPTION

OPERATION
- GATE CANNOT CHG STATE UNTIL PREVIOUS STAGE CHG STATE
- HOLD THE OUTPUT LOW SO NEXT STAGE NMOS IS OFF

PROS
- GLITCH FREE OPERATION
- CAN SIZE INVERTER TO DRIVE LARGE CAPACITIVE LOADS

CONS
- IF NMOS PRODUCES LOGIC 1 AT NODE A DURING EVALUATION, THEN NODE A IS SUBJECT TO LEAKAGE AND STATE CHANGE

KEEPER CIRCUIT
- IMPLEMENT KEEPER TO MAINTAIN STATE OF OUTPUT
- W/L SMALL TO NOT CHG OUTPUT
- CAN USE TWO LONG CHANNEL NMOS ALONG WITH PMOS TO REDUCE CAPACITANCE

NP, AKA ZIPPER
- SIMILAR, BUT REMOVE INVERTER
**DYNAMIC CIRCUITS**

![Dynamic Circuit Diagram]

**DYNAMIC* LATCH**
- "PSEUDO-STATIC"
  - IMPROVES NOISE IMMUNITY
  - INCREASE IN DELAY
  - CLK=L, D→DBAR
  - CLK=H, CAP KEEPS DATA

**DYNAMIC* REGISTER**
- BACK TO BACK LATCHES
- FLIP CLOCK FOR SLAVE STAGE
- CAN USE PASS GATES (NMOS ONLY) FOR SMALLER XTOR COUNT
- PROS
  - 4 VS. 10 GATES
  - SIMPLER
  - FASTER
  - LOWER POWER
- CONS
  - REFRESH NEEDED
  - DIODE LKG, SUBTHRESHOLD LKG
  - SUBJECT TO NOISE
  - DOES NOT TRACK DELTA VDD
  - CLOCK OVERLAP, D→QBAR

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*USES PARASITIC CAP IN CKT*