Baker Ch 13: Clocked Circuits

Topics:
1. Intro Foil
2. CMOS Transmission Gate Definition
3. Delay of TG
4. Applications of TG-Selector
5. Applications of TG-MUX
6. TG vs. Pass Transistor
7. Applications of TG-OR, XOR, XNOR
8. SR Latch-NAND, NOR
9. NAND Arbiter
10. Latch I/O Characteristics
11. Level Sensitive Latch
12. Edge-Triggered DFF
13. Edge DFF with Async SR, DFF Setup and Hold
Baker Ch 13: Clocked Circuits
CMOS Transmission Gate Definition

- TG passes a signal from IN to OUT or Z state, based on control signal
- Designer must create S and Sbar control signal
- Timing of S and Sbar are ideally the same, but it may have an impact
- NMOS passes 0 and PMOS passes 1
- Why? Hint: Think of definition of source in both NMOS and PMOS

![Schematic and Logic Symbol](image1.png)

**Figure 13.1** The transmission gate.

![Diagram](image2.png)

**Figure 13.2** The transmission gate with control signals shown.
Baker Ch 13: Clocked Circuits
CMOS Transmission Gate Delay

- TG has delay associated with passing signal from in to out
- RC delay is due to channel resistance of \((N \parallel P) C_{\text{load}}\)
- Control signals should be simulated through inverters to mimic Si driver
- \(R_n\) and \(R_p\) can be varied to modify delay

![Figure 13.3](image1.png)  
**Figure 13.3** TG circuit discussed in Ex. 13.1.

![Figure 13.4](image2.png)  
**Figure 13.4** TG circuit discussed in Ex. 13.2.
Baker Ch 13: Clocked Circuits

Applications of TG-Selector

• $Z = A$ or $B$ depending on $S$
• Output is always on, no high impedance state

![Diagram](image)

**Figure 13.6** Path selector.

<table>
<thead>
<tr>
<th>$S$</th>
<th>$Z$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$B$</td>
</tr>
<tr>
<td>1</td>
<td>$A$</td>
</tr>
</tbody>
</table>
Baker Ch 13: Clocked Circuits

Applications of TG-MUX

• MUX selects one output from multiple inputs
• Below example is 4-to-1 MUX
• What is the limitation of MUX input to output?
• DEMUX, flip inputs and outputs

![Diagram of a 4-to-1 MUX circuit](image)

<table>
<thead>
<tr>
<th>S1</th>
<th>S2</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A</td>
</tr>
</tbody>
</table>

Figure 13.8 Circuit implementation of a 4-to-1 MUX.
Baker Ch 13: Clocked Circuits
TG vs. Pass Transistor

- TG uses CMOS, Pass Transistor uses NMOS
- TG count = 16
- PT count = 8 or 6
- Why not do it all the time?
- What is the limitation?

![Figure 13.9 Transistor implementation of Fig. 13.8.](image1)

![Figure 13.10 MUX/DEMUX using pass transistors.](image2)
Baker Ch 13: Clocked Circuits

Applications of TG-OR, XOR, XNOR

• **OR:**  
  \( A=1, \ B=1, \ \text{PMOS}=\text{on}, \ \text{TG} \ \text{off}, \ \text{out}=A \ (1) \)  
  \( A=0, \ B=1, \ \text{PMOS}=\text{off}, \ \text{TG} \ \text{on}, \ \text{out}=B \ (1) \)  
  \( A=1, \ B=0, \ \text{PMOS}=\text{on}, \ \text{TG} \ \text{off}, \ \text{out}=A \ (1) \)  
  \( A=0, \ B=0, \ \text{PMOS}=\text{off}, \ \text{TG} \ \text{on}, \ \text{out}=B \ (0) \)

• Same ideas for XOR, XNOR

![Figure 13.11 TG-based OR gate.](image1)  

![Figure 13.12 TG implementation of XOR/XNOR gate.](image2)
• Basic latch used in DFF
• Set Rest Latch: S=1 output is 1, R=1 output is 0, S=R depends on type

Figure 13.13  Set-reset latch made using NAND gates.

Figure 13.14  Set-reset latch made using NOR gates.
Baker Ch 13: Clocked Circuits

NAND Arbiter

• Arbiter choose which input arrived first
• In1=0, In2=0: zero and anything is zero, output of NANDs are 1, OUT=0
• In1=1, In2=0: top output=0, keeps bot output=0, OUT2=0
• So the IN1 is the winner regardless of what IN2 does

Figure 13.15 An arbiter made using NAND gates.
• Latch I/O, ideally sharp transfer between states
• Butterfly curve represents the regions where both inverters contribute
• What is the issue with the characteristic?
• Metastability is not a desired state, want inverters to settle
• Can avoid the problem by various methods described in the text
Baker Ch 13: Clocked Circuits

Level Sensitive Latch

• Level sensitive latch changes state with a level change
• NMOS PG will lower D value
• I2 will battle with D change, increase the lengths, i.e., reduce the current
• Q output will change when clock is high, stores that value
• Delays going 0 → 1 different than from 1 → 0

Figure 13.18 A level-sensitive latch.

Figure 13.19 Simulating the level-sensitive latch in Fig. 13.18.
Baker Ch 13: Clocked Circuits
Improved Level Sensitive Latch

- Add in TG
- Delays between $1 \rightarrow 0$ and $0 \rightarrow 1$ are same
- Why?
Baker Ch 13: Clocked Circuits
Edge-Triggered DFF

- DFF changes state on the rising edge of the clock
- Delays exist, why?
- Very important to have clocks with quick rise times
- What is the issue if the clocks are slow?

**Figure 13.22** An edge-triggered D-FF.

D=0 (B=1) Latch Master

After rising edge of clock
After some delay

**Figure 13.23** Simulating the operation of the edge-triggered FF in Fig. 13.22.
Baker Ch 13: Clocked Circuits
Edge DFF with Async SR

• Set and Reset DFF, duplicate for CAD4
• Transfer of signal between D and B is setup time before clock latches
• Hold time is how long it must remain after clock is applied to latch
• \( t_h \) can be smaller as the \( t_s \) means \( t_h \) must be latched before next \( t_s \)

**Figure 13.24** An edge-triggered FF with asynchronous set and clear.

**Figure 13.25** Illustrating D FF setup time.

**Figure 13.26** Illustrating D FF hold time.