Class 01: Overview of IC Design Flow

Topics:
1. Introduction
2. Moore’s Law
3. Chip Process Flow
4. DPW: Motivation for Increasing Wafer Diameter
5. Chip Design Flow
6. Logic, Circuit, Models
7. Simulation
8. Layout Verification and Delay Extraction
9. Masks
10. Tests
In 1965, Gordon Moore was preparing a speech and made a memorable observation. When he started to graph data about the growth in memory chip performance, he realized there was a striking trend. Each new chip contained roughly twice as much capacity as its predecessor, and each chip was released within 18-24 months of the previous chip. If this trend continued, he reasoned, computing power would rise exponentially over relatively brief periods of time.

Moore's observation, now known as Moore's Law, described a trend that has continued and is still remarkably accurate. It is the basis for many planners' performance forecasts. In 26 years the number of transistors on a chip has increased more than 3,200 times, from 2,300 on the 4004 in 1971 to 7.5 million on the Pentium™ II processor.

Feature Size, 10um, 1um, 0.35um
aka Process Node
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Chip Process Flow (Wolf p.3)

Fig. 1-3 The fabrication process sequence of integrated circuits.
Fig. 1.1  (a) The same integrated-circuit die is replicated hundreds of times on a typical silicon wafer; (b) the graph gives the approximate number of $5 \times 5$ mm dice which can be fabricated on wafers of different diameters.
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Chip Design Flow (Wolf p.2)

Fig. 1-2 Steps required for the manufacture of very large scale integrated circuits (VLSI).

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Logic, Circuit, Models (Martin ch. 1)

A CMOS Inverter

* .MODEL nch NMOS
   + LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=1
   + VTO=0.8 DELTA=2.5E-01 LD=4.0E-08 KP=1.8E-04
   + UO=545 THETA=2.5E-01 RSH=2.1E+01 GAMMA=0.62
   + NSUB=1.4E+17 NFS=7.1E+11 VMAX=1.9E+05 ETA=2.2E-02
   + KAPPA=9.7E-02 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.0E-10
   + CJ=5.4E-04 MJ=0.6 CJSW=1.5E-10 MJSW=0.3 PB=0.99
*

* .MODEL pch PMOS
   + LEVEL=3 PHI=0.70 TOX=1.0E-08 XJ=0.20U TPG=-1
   + VTO=-0.9 DELTA=2.5E-01 LD=6.7E-08 KP=4.45E-05
   + UO=130 THETA=1.8E-01 RSH=3.4E+00 GAMMA=0.52
   + NSUB=9.8E+16 NFS=6.5E+11 VMAX=3.1E+05 ETA=1.8E-02
   + KAPPA=6.3E+00 CGDO=3.7E-10 CGSO=3.7E-10 CGBO=4.3E-10
   + CJ=9.3E-04 MJ=0.5 CJSW=1.5E-10 MJSW=0.3 PB=0.95
*

M1 3 2 0 0 CMOSN W=4u L=0.6u AS=7.2p PS=7.6u AD=7.2p PD=7.6u
M2 3 2 1 1 CMOSP W=5.5u L=0.6u AS=9.9p PS=9.1u AD=9.9p PD=9.1u
CL 3 0 0 0.05pF
*

VDD 1 0 3.3V
VIN 2 0 PULSE(0 3.3 0 100p 100p 5n 10n)
*
   .TRAN 0.05n 10n
   .PRINT TRAN V(2)
   .PLOT TRAN V(2)
*
   .DC VIN 0V 3.3V 0.01V
   .PRINT DC V(3) V(4) V(5)
   .PLOT DC V(5)
*
   .END

Figure 1.13 A CMOS inverter.

Figure 1.20 A CMOS inverter to be simulated using SPICE.
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Simulation (Martin ch. 1)

Figure 1.22 The transient analysis of the inverter of Fig. 1.20.
Figure 1.23 The d.c. transfer curve of the inverter of Fig. 1.20.

Analog Simulation - HSPICE, et.al.
Digital (Logic) Simulation - Verilog, et.al.
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Layout Verification and Extraction (Martin p.55)

Extraction - determining device and parasitic information
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Masks (Wolf p.4)

Metal X or PO

Fig. 1-4 (a) Example of the patterns transferred to a wafer during a seven-mask process sequence, and (b) Cross section of completed devices in a basic CMOS process.
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Testing (from experience)

In-Line Tests (Oxide Thickness, Poly Gate Width, Metal Sheet Resistance)
Parametric Tests (Ids, Vt, Tox, Gm, CT resistance, Comb/Serpent Yields)
Functional Tests (Memory Array R/W/E, Logic Patterns)
Product Tests (Full Speed, High Temp)
Qualification Testing (ESD, Latchup, Reliability, Package)
Customer System Tests (In-board testing)