Class 06: Device Physics III

Topics:
1. Introduction: NFET Operation
2. NFET Model and Cross Section with Parasitics
3. Final Results: IV Curves
4. Current Flow in a FET
5. Motivation: Understanding Spice Parameters
6. Terminology
7. Ideal Operation: Triode and Active Regions
8. Deriving the Linear Region
9. Deriving the Linear Region II
10. The Saturation Region
11. The Family of Curves for Id vs. Vds, Varying Vgs
12. The Threshold Voltage
13. The Body Effect
14. The SPICE Parameters
15. NFET Model and Cross Section with Parasitics
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NFET Model and Cross Section with Parasitics (Martin p.101)

- Goal is to understand the operation of an NFET shown in the model and cross section
- Last lectures covered the pn junctions of the source and drain, operation of the channel
- This lecture will cover the operation of the transistor as a whole
- Question: what type of component is $g_m \cdot V_{gs}$?
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Final Results: IV Curves (Martin p.97)

• IV curves explain how the transistor performs when biased in different configurations
• SPICE model explains these IV curves in terms of physics-based parameters
• This lecture will concentrate on ideal behavior (triode/active); non-ideal (short channel) later

• How many terminals in a NFET? Answer: 4 (S-G-D-Sub)
• The IV curve above assumes source and substrate are shorted
• The IV curve above assumes Id really means current from drain to source
• Why is it called source and drain, and where is the current flowing to/from?
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Current Flow in a FET (Martin p.87)

source

ground

drain
positive potential
Electron flow

Current flow

source is a “source of”

drain is “draining”

majority carriers flow

Current flow

NFET
electrons
source->drain
I_{drain->source}

PFET
holes
holes
source->drain
I_{source->drain}

Figure 3.12 A cross-sectional view of a typical n-channel transistor.
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Motivation: Understanding Spice Parameters (Martin p.121)

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- The ones not covered so far by lectures are: VTO, UO, LD, GAMMA
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Terminology (Martin c.3)

\( I_D \)  Drain current, usually implying drain-to-source current (what else would it be?)
\( I_{d\text{-lin}} \) (linear) - current in the linear region (triode region)
\( I_{d\text{sat}} \) (saturation) - current in the saturation region (active region)
\( \mu_n \) Mobility of electrons
\( W \) Width of channel
\( L \) Length of channel
\( C_{ox} \) Capacitance of channel oxide
\( V_{gs} \) Gate to source potential
\( V_{tn} \) Transistor threshold for n-type
\( V_{ds} \) Drain to source potential
\( V_{ds\text{-sat}} \) Drain to source potential in the saturation regime
\( V_{eff} \) \( V_{gs} - V_{tn} \), which gives the voltage amount above or below threshold
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Ideal Operation: Triode and Active Regions (Martin p.94)

Three regions of operation:
• Linear or Triode Region  
  \[ V_{ds} \ll V_{eff} \]  
  channel inverted
• Saturation or Active Region  
  \[ V_{ds} > V_{eff} \]  
  channel pinched off
• Transition region  
  \[ V_{dg} \sim V_t \text{ or } V_{ds} \sim V_{eff} \]  
  beginning of pinch off
Similar to a resistor \( J = \sigma E \) where the conductivity is \( \sigma = qn\mu_n \) \( n \) is density/volume and \( \mu_n \) is the mobility of the carrier.

This gives a current density of \( J = qn\mu_n E \)

The total current flowing through a cube of dimensions \( W, L, H \) is \( I = JWH \)

The voltage drop along the direction of current flow is \( dV = E(x)dx \)

Combining the above gives \( q\mu_n WH n(x) dV = I dx \)

where \( n \) is a function of \( x \)

If one expresses \( n(x) \) as a function of charge density per unit square \( Q_n(x) = qHn(x) \)
gives the relationship \( \mu_n WQ_n(x) dV = I dx \)

Since the voltage in the channel is not constant, one needs to relate the gate-source, threshold, and channel potentials to the charge in the channel through \( Q = CV \). This formulates the vertical and horizontal relationships.

\[
Q_n(x) = C_{ox} [V_{GS} - V_{ch}(x) - V_{tn}]
\]
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Deriving the Linear Region II (Martin c.3 Appendix)

Integrating the equation from $0 < dV < V_{ds}$ and from $0 < dx < L$ gives:

$$
V_{DS} \int_{0}^{L} \mu_n W C_{ox} [V_{GS} - V_{ch}(x) - V_{tn}] dV_{ch} = \int_{0}^{L} I_D dx
$$

Solving for $I_d$ gives the linear region:

$$
I_D = \mu_n W C_{ox} \left[ (V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right]
$$

For very small $V_{ds}$ (i.e., $V_{ds} \ll V_{eff}$):

$$
I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) V_{DS} = \mu_n C_{ox} \frac{W}{L} V_{eff} V_{DS}
$$

Substituting the charge density in the channel into the current equation:

$$
\mu_n W Q_n(x) dV = I dx
$$

gives

$$
\mu_n W C_{ox} [V_{GS} - V_{ch}(x) - V_{tn}] dV_{ch} = I_D dx
$$
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The Saturation Region (Martin p.93)

What causes the current to saturate?
- As the drain voltage increases, the depletion region around the drain increases
- As the depletion region increases, the number of free carriers at the drain decreases
- The voltage at the drain is opposing the voltage from the gate, so the Vgd falls below Vtn
- This is referred to as pinch-off, since the channel carrier density is pinched
- One can then substitute \( V_{ds} = V_{gs} - V_{tn} \) into the linear equation to obtain

\[
I_D = \frac{\mu_n C_{ox} W}{2} \frac{V_{gs} - V_{tn}}{V_{ds}}^2
\]
As one increases the gate to source bias, the location of the pinch off increases since you now have more carriers in the channel.

Short channel effects (to be discussed later):
velocity saturation
mobility degradation
reduced output impedance
hot-carrier effects
There are many factors that affect the gate-source voltage at which the channel becomes conductive:

1. The work-function difference between the gate material and the substrate material.
2. The voltage drop between the channel and the substrate required for the channel to exist.
3. The voltage drop across the thin oxide required for the depletion region with its immobile charge to exist.
4. The voltage drop across the thin oxide due to unavoidable charge trapped in the thin oxide.
5. The voltage drop across the thin oxide due to implanted charge at the surface of the silicon. The amount of implanted charge is adjusted in order to realize the desired threshold voltage.

\[
V_{t\text{-native}} = \phi_{MS} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}
\]

(1) (2) (3) (4)

• The Vt implant is the “knob” used to control the behavior of the transistors
• Everything else in the equation is fixed for a given technology
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The Body Effect (Martin p.98, c.3 Appendix)

As the bias on the substrate is made negative with respect to the source ($V_{sb}$: $V_{source}$-to-substrate is positive), the p-type carriers are pulled away from the surface, increasing the depletion depth. This causes the channel to become more difficult to invert, shifting the $V_t$ to a more positive value. The zero substrate bias is given as $V_{t0}$, and the body effect modifies the $V_{t0}$ as:

$$V_{t0} = V_{t0-0} + \gamma \left( \sqrt{V_{SB}} + \sqrt{2\phi_F} - \sqrt{2\phi_F} \right)$$

$$\gamma = \frac{\sqrt{2qN_AK_s\varepsilon_0}}{C_{ox}}$$

This modifies the IV curve as:

$$I_D = \mu_n \frac{W}{L} C_{ox} \left[ (V_{GS} - V_{t0})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\alpha \equiv 1 + \frac{\gamma}{2\sqrt{V_{SB} + |2\phi_F|}}$$
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The SPICE Parameters (Martin p.121)

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We have now discussed all of the above, except:
Ld is related to the pinch-off region, how far the drain is located underneath the gate
MJ, MJSW which are the non-abrupt junction parameters for a pn junction
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NFET Model and Cross Section with Parasitics (Martin p.101)

Transconductance: $g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn})$

Influence of body effect: $g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{tn}} \frac{\partial V_{tn}}{\partial V_{SB}}$

Rds is the drain to source resistance