Class 08: NMOS, Pseudo-NMOS

Topics:

• 02 NMOS Logic Gates
• 03 NMOS Logic Gates
• 04 Pseudo-NMOS
• 05 Pseudo-NMOS
• 06 Transistor Equivalency
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NMOS (Martin c. 1)

- nMOS Inverter with resistive load

- switch level model

- Including transistor resistance

- nMOS Inverter with depletion load

- nMOS NOR gate

- nMOS NAND gate

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NMOS (Martin c. 1)

- General nMOS schematic
  - single load transistor
  - parallel and series nMOS transistor to complete the complement of the desired function
    i.e., they determine when the output is low “0” rather than high “1”

Examples: depletion-load nMOS logic
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Pseudo-NMOS (Martin c. 4)

• NMOS Common-Source Amplifier with current source load and load capacitor

\[ V_{\text{eff}} = V_{\text{gs}} - V_{t} \]
\[ V_{\text{ds}} = V_{\text{gs}} + V_{\text{dg}} \]

at saturation, \( V_{\text{dg}} = -V_{t} \)

Valid if:
\[ V_{\text{eff}} = |V_{\text{ds}}| > |V_{\text{gs}}| - |V_{t}| \]

- want drain at least \( V_{t} \) from gate

• Pseudo-NMOS inverter with PMOS load

* Choose W/L so that:

\[
(W/L)_1 = \frac{(W/L)_2}{2}
\]

* Choose \( V_{\text{bias}} \) in between \( V_{DD} \) and ground

Q2 always on since \( |V_{\text{gs}}| > |V_{tp}| \)

Q2 in saturation if (for \( V_{DD} = 3.3 \))

\[ |V_{\text{ds}}| > |V_{\text{eff}}| > |V_{\text{gs}}| - |V_{t}| \]
\[ V_{\text{DD}} - V_{\text{out}} > |V_{\text{gs}}| - |V_{t}| \]
\[ V_{\text{out}} < V_{\text{DD}} - |V_{\text{gs}}| + |V_{t}| \]
\[ V_{\text{out}} < 1.65 + V_{t} < 2.45 \]

Q1 in saturation if

\[ V_{\text{gs}} = V_{\text{in}} > V_{t} \]
\[ V_{\text{ds}} > V_{\text{eff}} > V_{\text{gs}} - V_{t} \Rightarrow V_{\text{out}} > V_{\text{in}} - V_{t} \]

* Power Dissipation:

Output low (Vin is high):
\[ P = I_{L} \times V_{DD} \]

Output high (Vin is low):
\[ P = 0 \]

Average static dissipation:
\[ P = \frac{1}{2} \times I_{L} \times V_{DD} \]

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Pseudo-NMOS (Martin c. 4)

**XOR Logic in Pseudo-NMOS**

\[ y = x_1 \oplus x_2 = x_1 \overline{x_2} + \overline{x_1} x_2 \]

\[ = x_1 x_2 + x_1 \overline{x_2} \]

\[ = x_1 x_2 + x_1 \overline{x_2} \quad \text{remember:} \]

\[ a' + b' = (ab)' \]

\[ a b' = (a + b)' \]

**Evaluating functions from schematics**

1. start with any transistor connected to ground
2. OR parallel and AND series transistors, combining all subnets in same manner
3. do again for each transistor connected to ground, and combine groups
4. take the compliment of the result

**Example:**

\[ V_{out'} = [x_1 (x_4 + (x_2 + x_3) (x_5 + x_6 + x_7)) ] \]

\[ V_{out} = [x_1 (x_4 + (x_2 + x_3) (x_5 + x_6 + x_7)) ]' \]
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Transistor Equivalency (Martin c.2, c.4)

- Scaling both W and L
  
  \[
  Q_1 \quad \text{W/L} \quad \equiv \quad Q_{eq} \quad \text{(KW)/(KL) for any K}
  \]
  
  - transistors act the same (to first order)

- Series Transistors
  
  \[
  Q_2 \quad \text{W/L}_2 \quad \equiv \quad Q_{eq} \quad \text{W/(L}_1 + \text{L}_2)\]
  
  - effectively increases L

- Parallel Transistors
  
  \[
  W/L_1 \quad \equiv \quad (W_1 + W_2)/L
  \]
  
  - effectively increases W

Example: Parallel Transistors

Figure 2.17: (a) layout, (b) schematic direct from layout, (c) simplified schematic