Class 09: CMOS Gates

Topics:

1. CMOS Inverter
2. CMOS Gate Examples
3. Threshold Voltage
4. Inverter Gain at Vin=Vth
5. Transient Response
6. Effect of Transistor Sizes on Transient Response
7. Power Dissipation
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CMOS Inverter (Martin c.1, Weste p.8)

- Similar to NMOS, a CMOS inverter is realized by the replacement of the load transistor with a PMOS network.
- NMOS is used to pull the output low (pull-down), NMOS is used to pull the output high (pull-up). Why?
  - The NMOS (PMOS) source should be as close to VSS (VDD) as possible (body-effect, volt drop across channel)
- During static operation, either the NMOS (Vin=0) or the PMOS (Vin=1) is off, so no DC path to ground
- During dynamic (switching) operation, power is dissipated
- Parallel components in NMOS translate into series components in PMOS
- Series components in NMOS translate into parallel components in PMOS

![CMOS Inverter Diagram]

**TABLE 1.1 The Output Logic Levels of N-SWITCHES and P-SWITCHES**

<table>
<thead>
<tr>
<th>LEVEL</th>
<th>SYMBOL</th>
<th>SWITCH CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strong 1</td>
<td>1</td>
<td>P-SWITCH gate = 0, source = VDD</td>
</tr>
<tr>
<td>Weak 1</td>
<td>1</td>
<td>N-SWITCH gate = 1, source = VDD or P-SWITCH connected to VDD</td>
</tr>
<tr>
<td>Strong 0</td>
<td>0</td>
<td>N-SWITCH gate = 1, source = VSS</td>
</tr>
<tr>
<td>Weak 0</td>
<td>0</td>
<td>P-SWITCH gate = 0, source = VSS or N-SWITCH connected to VSS</td>
</tr>
<tr>
<td>High impedance</td>
<td>Z</td>
<td>N-SWITCH gate = 0 or P-SWITCH gate = 1</td>
</tr>
</tbody>
</table>

![Output Levels Diagram (a) and (b)]
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CMOS Gate Examples (Martin c1)

NOR

When a=1 and b=0:
- Q1 is off, Q2 is on
- Q3 is on, Q4 is off
No DC path (Q4 off)

NAND

A | B | Vout
---|---|---
0 | 0 | 1
0 | 1 | 1
1 | 0 | 1
1 | 1 | 0

Parallel p-ch (a+b)
Series n-ch (ab)

Compound Logic (AOI)

Q1n-Q2n in series complemented by Q1p-Q2p in parallel
Q3n in parallel of Q1nQ2n complemented by Q3p in series with Q1pQ2p

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For calculating inverter threshold (not the same as transistor threshold), it is defined as the voltage where \( V_{\text{in}} = V_{\text{out}} \).

When \( V_{\text{in}} = V_{\text{out}} \), the NMOS has \( V_{\text{dg}} = 0 \), which means transistor is in the saturation region, since \( V_{\text{ds}} = V_{\text{gs}} - V_{\text{tn}} = V_{\text{eff}} \) is where saturation occurs (onset of pinch-off).

For saturation region:

\[
I_{D-1} = \frac{\mu_n C_{\text{ox}} W}{2 L} (V_{\text{th}} - V_{\text{tn}})^2
\]

\[
I_{D-2} = \frac{\mu_p C_{\text{ox}} W}{2 L} (V_{\text{DD}} - V_{\text{th}} + V_{\text{tp}})^2
\]

Equating the NMOS and PMOS currents, taking the square root, and solving for \( V_{\text{th}} \) gives the following relationship:

\[
V_{\text{th}} = \frac{V_{\text{tn}} + (V_{\text{DD}} + V_{\text{tp}}) \sqrt{\mu_p (W/L)_2 / \mu_n (W/L)_1}}{1 + \sqrt{\mu_p (W/L)_2 / \mu_n (W/L)_1}}
\]

- \( V_{\text{th}} \) is proportional to square root of mobilities
- Later will be shown that optimal \( W_p/W_n \) also is related by square root of mobilities

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Inverter Gain at \(V_{\text{in}}=V_{\text{th}}\) (Martin c4.4)

Small signal equivalent circuit is used by setting DC power supplies to zero, and the body effect is ignored.

Since the NMOS and PMOS look identical, they can be combined to give the gain when \(V_{\text{in}}=V_{\text{th}}\):

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = -(g_{m-1} + g_{m-2})(r_{ds-1} \parallel r_{ds-2})
\]

Ignoring body effect, and solving for \(V_{\text{out}}/V_{\text{gs}}\):

Small signal model of inverter
From Chapter 1, the transient response of an ideal node was given as:
\[ \Delta t = C_p \Delta V_n / I_{ch} \]

where \( V_n \) is the charging node voltage, \( C_p \) is the parasitic capacitance on the node, and \( I_{ch} \) is the charging node current. Simplifying the charging current as:
\[ I_{ch} = \frac{V_{DD} - V_n}{R_L} \]

and solving for \( t_2 - t_1 \) gives (when the voltage is \( V_{DD} \))
\[ \Delta t = R_L C_p \ln \left\{ \frac{(V_{DD} - V_{n1})}{(V_{DD} - V_{n2})} \right\} \]

As with the pseudo-NMOS, the equivalent resistance given by the \( I_d \) vs. \( V_{out} \) curve can be approximated:
\[ R_{eq} = 2.5 / \left\{ \mu_n C_{ox} (W/L) (V_{DD} - V_{tn}) \right\} \]

Where does the 2.5 vs. 2.0 factor come from?

This gives, for a 70% change in voltage,
\[ t \sim 1.2 R_{eq} C_L \]

Where does 1.2 come from? Assume \( V_{dd}=3.3 \), \( V_{n1}=0 \) (initial voltage), and \( V_{n2}=2.31 \).
So where does 2.31 come from? \( V_{n2}=2.31 \) comes from 70% of voltage swing (3.3V).
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Effect of Transistor Sizes on Transient Response (Martin c4.4)

Consider a inverter that is loaded by two identical inverters. There are two load capacitances to consider:
1) junction capacitances of the drains of the inverter 1
2) gate capacitances of inverters 2 and 3

The approximate capacitance of gate to channel is given as
\[ C_{gs} = W L C_{ox} \]
This gives a load capacitance on inverter 1 due to inverters 2 and 3 as
\[ C_L = 2 C_{ox} L ( W_n + W_p ) \]

Increasing widths increase the gate capacitance by lowering the equivalent resistance, so net effect of W on transient response can be neglected. This assumes short channel effects are ignored. So delay can be optimized by optimizing the W/L ratio of the p-ch to the W/L ratio of the n-ch.

The average delay due to inverter 2 and 3 is:
\[ t \sim 1.2 \left( R_{eq1} + R_{eq2} \right) C_L / 2 \]

Assuming Vdd-Vtn = Vdd + Vtp:
\[ t_{AV} = \frac{3L^2}{(V_{DD} - V_{tn}) \mu_n} \left( 1 + \frac{W_p}{W_n} \right) \left( 1 + \frac{\mu_n W_n}{\mu_p W_p} \right) \]

To optimize for Wp/Wn:
\[ \frac{\partial t_{AV}}{\partial (W_p/W_n)} = \frac{3L^2}{(V_{DD} - V_{tn}) \mu_n} \left( 1 - \frac{\mu_n W_n}{\mu_p W_p} \right)^2 \]

\[ T_{proc} = \frac{L^2}{(V_{DD} - V_{tn}) \mu_n} \]

\[ \left( \frac{W_p}{W_n} \right)_{opt} = \sqrt{\frac{\mu_n}{\mu_p}} \]

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Power Dissipation (Martin c4.4)

Power Dissipation is comprised of three components:
1) Static 2) Dynamic 3) Short Circuit

1) Static Power Dissipation
-due to reverse bias junction leakage

2) Dynamic Power Dissipation

So, in any one period, the total energy dissipated is:

\[ E_T = C_L V_{DD}^2 \]

The average power is Energy per Unit Time (period):

\[ P_{dyn-avg} = \frac{C_L V_{DD}^2}{T} = C_L V_{DD}^2 f_{clk} \]

3) Short Circuit (Direct Path) Power Dissipation

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