Class 15: Input / Output Circuits

Topics:
1. Introduction
2. Input Protection
3. Input and Output Circuits
4. Input and Output Circuits
5. Input and Output Circuits
6. Input and Output Circuits
7. Input and Output Circuits
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Why does one need protection on inputs pads?
HBM ESD

If an oxide has a resistance of $1 \times 10^9$ ohms, what current exists at 1kV?
$I = \frac{1e3}{1e9} = 1e-6 \text{ C/s}$
$Q = \frac{1e-6 \text{ C/s}}{1.602e-19 \text{ C/e-}} \approx 6e12 \text{ e-/s}$
-does not take very much charge to be placed on a gate to charge to 1kV

When charge is present, the desire is to shunt it to ground or power
Simple input protection circuit

![Diagram of input protection circuit]

**Figure 6.10** A commonly used CMOS input protection circuit.

What is this preventing?
Why are the diodes in the direction they are?

- Voltage clamped to ~GND or ~VDD
- Resistance is referred to as an ESD resistor. What is its function?
- Do you want R to be large or small? How is it formed?
Alternative protection circuit using field transistor

E-fields: \( \frac{1.8V}{30A} = \frac{1.8V}{30 \times 10^{-10} m} = 0.06 \times 10^9 \text{ V/m} = 6 \times 10^8 \text{ V/m} \)

Field threshold on the order of 20V
Driving capacitive loads:
• Capacitive loads at the chip I/O much larger than internal cap
• 1-30pF load translates into 500um to 1000um xtor widths
• To get this equivalent width, a chain of inverters is used

• Ideal situation, subsequent size increases by e (2.72)

![Diagram of an output driver](image)

**Figure 6.12** A typical output driver.

• What are the p and n widths shown above?
Tri-State Outputs: 0, 1, Z

Simple example:

Enable   Output
“0”      Z
“1”      Data

Why is this configuration not desirable?
Output driven through what?
Class 15: Input / Output Circuits
Input and Output Circuits (Martin p.274-7)

Another approach:

<table>
<thead>
<tr>
<th>Enable</th>
<th>Data</th>
<th>in-a</th>
<th>in-b</th>
<th>Q1(p)</th>
<th>Q2(n)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>off</td>
<td>off</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>off</td>
<td>on</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>on</td>
<td>off</td>
<td>VDD</td>
</tr>
</tbody>
</table>

Inverters add more drive current
More efficient approach:

<table>
<thead>
<tr>
<th>Enable</th>
<th>Q5(n)</th>
<th>Q6(p)</th>
<th>Q4(p)</th>
<th>Q8(n)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>N1-N2 shorted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(thus Q3 connected to Q7 and Q4 connected to Q8, which looks like an inverter)</td>
</tr>
<tr>
<td>0</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>N1-&gt;VDD, N2-&gt;GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Q1, Q2 off: High-Z</td>
</tr>
</tbody>
</table>

Figure 6.15 An efficient realization of the circuit of Fig. 6.14.