Class 17: Design Margins

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Motivation

Why build design margins into a design?

What are the variables that should be considered?

What does it mean when a chip “fails”?

How many steps does it take to make a chip?

Who makes the decision whether a chip is good or not?

How do reliability, yield, and design margin interact?
Metal conductors must be sized correctly to account for the following:
• Metal migration, a.k.a., electromigration
• Power supply noise and integrity (correct voltage levels)
• RC Delay

Electromigration
• Effect caused by finite amount of electrons in a conductor
• Sometimes referred to as migration due to “electronic wind”
• Increases when the current increases and/or temperature increases
• Dependent on crystal structure of conductor
• Increases over regions of large step sizes, such as ?
• It is a wearout mechanism, therefore a reliability issue
• Can be caused by Si precipitates which happen in Al:Si films
  • Add Cu, Ti to Al, or use other conductors (W, Mo)
  • Layer the film, with addition of Ti, W, or Mo layer in between Al layers
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Electromigration (Wolf p.265)

Electromigration

Fig. 4-51 (a) Schematic drawing of stress-induced voids in Al interconnect lines. (b) SEM photo of such a void. (c) Schematics of one proposed formation-mechanism of slit-like voids.260 (© 1985 IEEE).
Power supply noise and integrity (correct voltage levels)

- When a cell has a clock transition, power is needed for the transition. Why?

- SPICE plots showing the affect of load on current draw from power supplies. Plots are for short-circuit and capacitive currents.
Power supply noise and integrity (correct voltage levels)

Given the following:
- Clock buffer running at 50-MHz
- Drives a 100pF load
- Maximum electromigration of 0.5mA/µm
- Buffer is 500µm from the power and ground pads
- Power supply is 5V
- Metal sheet is 0.05 Ω/sq
- $t_r$ and $t_f$ of clock is 50ns

Find
- Conductor width for power/ground bus to meet EM
- Ground bounce
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Power and Ground Bounce (Weste p.239-240)

Power supply noise and integrity (correct voltage levels)

Capacitive power dissipated:
\[ P = CV_{DD}^2f \]
\[ = 100 \times 10^{-12} \times 25 \times 50 \times 10^6 \]
\[ = 125 \text{ mW} \]
\[ I = 25 \text{ mA} \]

Given a 5V power supply, 100pF load, 50-MHz clock
So, 25mA / 0.5 mA/µm= 50µm width. For margin, choose 100µm.

Ground bounce:
\[ R = \frac{500}{100 \times .05} \]
\[ = 5 \text{ squares} \times .05 \Omega/\text{sq.} \]
\[ = .25\Omega \]
\[ IR = \frac{C_dV}{dt} \quad R = \frac{100 \times 10^{-12} \times 5}{1 \times 10^{-9} \times .25} \]
\[ = 125 \text{ mV (also see Section 5.5.16)} \]

Given 500µm length of bus, 100µm width from above, 0.05 sheet resistance, load of 100pF, dV/dt of 5V/1ns
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Conductor Sizing - RC Delays (Weste c.4)

RC Delay
• Can be modeled in terms of a distributed network

To alleviate delays, can add buffers to critical areas for timing issues, or add more power pins for voltage sensitive issues
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Conductor Sizing - RC Delays (Weste p. 198)

RC Delay
Capacitance as a function of spacing, height, and width:

![Diagram showing capacitance as a function of normalized conductor spacing, with different line styles for various widths.](image)
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Contact Replication (Weste c.4)

Current will tend to crowd if the resistance across the conductor is not uniform

If the current flow does NOT change direction

If the current flow does change direction
A bus (or any other interconnect) can be modeled as a capacitor from conductor to ground \((C_b)\).

If there are gates on this bus that are sampled, the gates that are sampled can be modeled as \(C_s\).

The charge on each capacitor is:

\[
Q_b = C_b V_b, \quad Q_s = C_s V_s.
\]

The total charge is given as the sum of the two:

\[
Q_T = C_b V_b + C_s V_s.
\]

The total capacitance is:

\[
C_T = C_b + C_s.
\]

When the switch is closed, the total voltage on the bus:

\[
V_R = \frac{Q_T}{C_T} = \frac{C_b V_b + C_s V_s}{C_b + C_s}.
\]

Ex., if \(V_b = V_{DD}\) and \(V_b \gg V_s\), then it is a voltage divider:

\[
V_R = V_{DD} \left[ \frac{C_b}{C_b + C_s} \right].
\]
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Charge Sharing (Weste c.4)

Charge sharing:

Given the following:
• A pre-charged bus has a load of 10pF
• At some point in a clock cycle, 64 registers (with a load of 0.1pf) have their inputs turn on

Find
• The change in the pre-charge voltage

Here \( C_b = 10pF \)
\( C_s = 64 \times 0.1pF = 6.4pF \)
\( V_{DD} = 5V \)

Hence
\[
V_R = 5 \times \frac{10}{10 + 6.4} = 3.05 \text{ volts (change in voltage is 1.9V).}
\]
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Temperature, VDD Effects (Weste c.4)

Variation of $I_d$s vs. Temperature

<table>
<thead>
<tr>
<th>Typical</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min</td>
<td>max</td>
</tr>
<tr>
<td>-40°C</td>
<td>85°C</td>
<td>-55°C</td>
</tr>
</tbody>
</table>

Die Temperature $T_j$:

$$T_j = T_a + \theta_{ja} \times P_d$$

where

- $T_j$ = the junction temperature in °C (temperature of the chip itself)
- $T_a$ = the ambient temperature in °C (temperature of surrounding air)
- $\theta_{ja}$ = the package thermal impedance, expressed in °C/watt
- $P_d$ = the power dissipation.

VDD +/- 10%
4.5 < VDD < 5.5
3.0 < VDD < 3.6

How does speed vary with VDD?
How does power vary with VDD?
What is 6 sigma?
- If a process is controlled to +/- 3 sigma, then only 0.26% of parts will fail
- If one artificially limits the distribution, then one can guarantee a certain robustness
Corners based on performance:
Fast  Nominal  Slow

Corners based on independent transistors:
P
fast  nominal  slow
fast
N  nominal  slow

Corners based on Ids-Vt considerations:
Vt
low  high
fast
Ids  nominal  slow

Worst-power, high-speed:
low T, high-VDD, fast-n, fast-p

Worst-speed:
high T, low-VDD, slow-n, slow-p

For digital parts, one would use
worst-power, high-speed at some
margin of +10% nominal frequency

Why is part faster at lower T?
Why is part slow at higher T?