Class 18: Memories-DRAMs

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Advantages and Disadvantages of DRAMs (Martin c.11, Wolf c.8)

Advantages:
• Very dense
• Cost per bit is low
• Driver of new technologies

Disadvantages:
• Process complexity
• Design complexity
  • Read and Refresh periodically
  • External circuitry more complicated
• Profit
  • Only one US manufacturer of DRAMs (Micron)
Static logic circuits
• a.k.a. MOS combinational logic
• no need for clocks
• static registers (flip-flops)

Dynamic logic circuits
• clocked logic
• faster operation
• greater circuit density
• reduced power dissipation
• dynamic registers
• stored charge undergoes leakage

How long can a charge remain on a node?
• Room temperature, approximately 10ms

How to take advantage of this charge storage effect?
• If one could refresh the charge before 10ms, dynamic registers could be a memory element
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Evolution of DRAMs (Martin c.11, Wolf c.8)

• 1968: DRAM patented by Dennard (IBM), using 1-T design
• 1970: First commercial DRAM (Intel), using 3-T design
• First commercial 1-T cell
  • 8um feature size
  • 1280 um2 area
  • 4-kbit NMOS
• Present commercial DRAMs (Seimens/IBM)
  • 0.18um feature size
  • 1-Gbit
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Basics of DRAMs (Martin c.11, Wolf c.8)

Storing a “0”:
• storage capacitor discharged by
  • word line to high (3.3V-on)
  • bit line to low (0V)
  • word line to low (0V-off)

Storing a “1”:
• storage capacitor charged by
  • word line to high (3.3V-on)
  • bit line to high (2.2-3.3V)
  • word line to low (0V-off)
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Basics of DRAMs (Martin c.11, Wolf c.8)

Reading issues
- storage capacitor 1/10 of parasitic bit line cap
- no differential bit lines
- noise
- destructive reads

Reading “1” or “0”
- pre-charge bit line to 3.3V
- access transistor turned on
- when “1” is stored, no change to BL voltage
- when “0” is stored, BL voltage changes ~0.2V
- no BL reference
- noise is same magnitude of sense voltage

How to overcome sensing issues
- Need to generate a comparison voltage
- Dummy cells are used
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Write Operation (Martin c.11, Wolf c.8)

Write a “1”
• VDD to BL, and VDD to WL
• Surface potential at the storage node and at the transfer gate is less than VDD
• electrons flow from storage to BL
• capacitor is in what area of operation for CV?
• WL goes to 0V

Write a “0”
• 0V to BL, and VDD to WL
• Surface potential at the storage node is greater than 0V
• electrons flow from BL to storage node
• capacitor is in what area of operation for CV?
• WL goes to 0V
During normal operation
• SA outputs D and D pre-charged to VDD through Q1, Q2 (Pr=1)
• reference capacitor, Cdummy, connected to a pair of matched bit lines and is at 0V (Pr=0)
• parasitic cap $C_p2$ is ~ 24 Cs, which sets up a differential voltage LHS vs. RHS
due to rise time difference
During read operation
• p-ch load transistors (Q1,Q2) and ref transistor turned off (Pr=1, Pr=0)
• Read goes high, Q6/Q7 on, and Q5 on
• SA is now connected to 1 BL (SBL) on LHS, and 2 BL (DBL) on RHS
• SA outputs (D, D) become charged, with a small difference LHS vs. RHS
• SBL feeds to Q4, which in turn feeds Q3 gate - positive feedback, but not to VDD
• SBL is brought up to VDD-Vtn if initially stored a “1”; grounded if initially stored a “0”
During read operation:
- both BL pre-charged to VDD/2
- cell being read is one of the BL, dummy cell is other
- Q1, Q2 turned on
- VDD/2 achieved by one BL to VDD, other to 0V and connect through Q7
- pre-charge also eliminates any existing stored charge

Refresh
- one SA per 4 BL
- necessary regardless of whether accessing the cell
- Assume for 256 cells
  - memory cycle time is 20ns
  - each 1ms all of the cells must be refreshed
  - total refresh time is 256 x 2e-8 = 5.12us
  - cannot use memory 5.12us / 1ms = 0.50% of time
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DRAM Cells (Martin c.11, Wolf c.8)
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DRAM Trench Capacitor (Martin c.11, Wolf c.8)

- Si area reduction of trench vs. planar capacitor ~ factor of 18
- 4um deep trench, surface 0.87um x 2.4um, capacitance of 40fF
- trench similar to STI except:
  - thin ox required
  - polysilicon fill
  - sidewall doping
- Issues
  - corner rounding, bottom uniformity
Access transistor needs large effective gate voltage to avoid voltage drop
voltage level booster accomplished by use of a charge-pump driver
Q2 is a capacitor with large W and L
Pr high, Q1 and Q4 on, Q3 off, thus Q2 is close to VDD (VDD-Vtn)
Pr low, Q1 and Q4 off, Q3 on, thus bottom plate of Q2 at VDD, top plate changes to a value above VDD
Used in level translator (Q5-Q10) and WL driver (Q11-Q12)