Class 19: Memories-EEPROMs and FLASH

Topics:

1. DA2/DP Issues
2. Types of Non-Volatile Memories
3. EEPROMs / Flash
4. EEPROMs
5. FLASH
6. Baising
7. Embedded FLASH Chip

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Types of Non-Volatile Memories

ROM
- read only memory
- fusible-link ROM

EPROM (a.k.a. UV PROMS)
- electrically (erasable) programmable read only memory
- UV shown through quartz window to erase

EEPROM (E^2)
- electrically erasable programmable read only memory

FLASH
- EEPROM-like, but entire array erasable at once

SONOS
- Silicon Oxide Nitride Oxide Semiconductor

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EEPROMs / Flash (Martin c.11)

Realized by using a floating gate transistor, in a double poly process

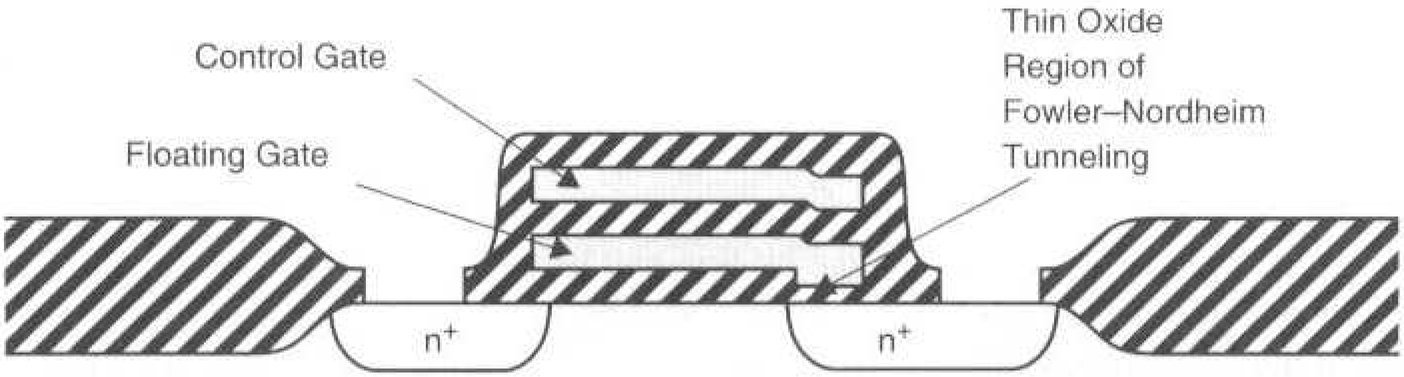

Figure 11.34 An EPROM cell that uses Fowler–Nordheim tunneling for charge transfer to floating gate.

Advantages:

- user can readily change memory stored, as opposed to ROM
- flexible in terms of configurations

Disadvantages

- expensive process due to extra masks (dnwell, hvnwell, hvpwell, fpoly, etc.)
- design issues (programming, erasing, reading)

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EEPROMs (Martin c.11)

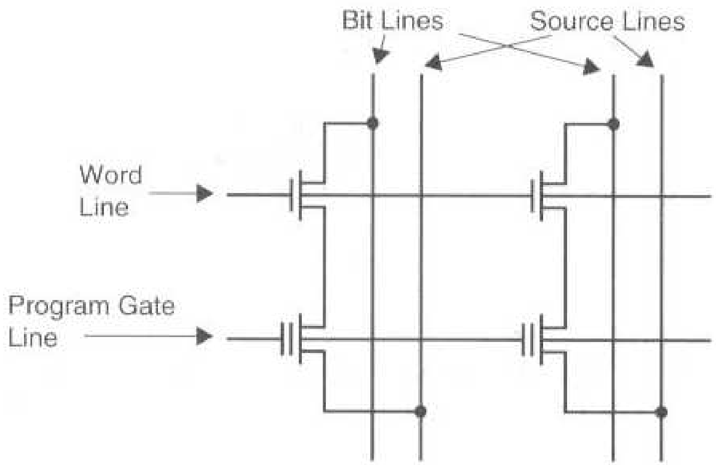

Figure 11.35 Two adjacent memory cells of a common EEPROM memory array.

Program:
- Individual cell selected using pass transistor
- Source and BL low; PG put at high voltage (12V)
- Electrons transferred from SD region to floating gate, thus shifting Vt

Erase:
- Individual cell selected using pass transistor
- WL and BL high (12V); PG low (0V); SL floating
- Electrons transferred from floating gate to D, thus shifting Vt

Read:
- WL and PG held at VDD
- If PG has stored charge, the gate is below the Vt and no current flows
- If PG has no charge, the gate is above the Vt and current flows

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FLASH

Program:

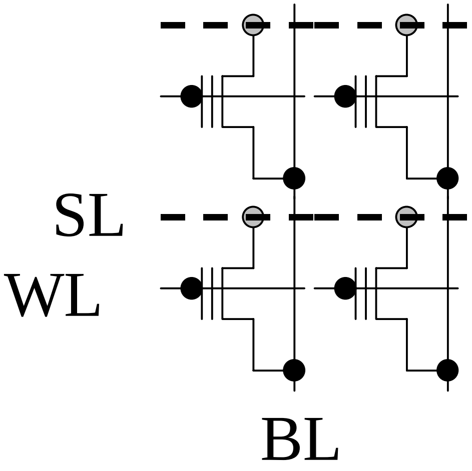
- SL 0V; BL VDD; WL put at high voltage (12V)
- Current flow from S to D, injected to floating gate, thus shifting V
- HCI type programming

Erase:

- SL VDD; WL negative voltage; BL floating
- Electrons transferred from floating gate to source, thus shifting Vt

Read:

- SL 0V; WL VDD; BL 1V
- If PG has stored charge, the gate is below the Vt and no current flows
- If PG has no charge, the gate is above the Vt and current flows



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Baising

	WL	BL	SL	Body
PGM-HCI	MV	MV	GND	GND
PGM-FN (channel)	HV	float/gnd	float/gnd	GND
RD	VDD	SA	GND	GND
EE-FN1 (source)	GND	float	HV	float
EE-FN2 (channel)	NV	float/gnd	float/gnd	GND

Programming:

FN: Fowler-Nordheim tunneling

•electrons tunnel through tox potential barrier

•traps in tox cause electronic charge to remain in oxide

•12V Vgs, 0V drain and source, 10^7 V/m

•low current

•good process control over tox needed

HCI: Hot Carrier Injection

•energetic electrons surmount tox potential barrier

•creation of “hot holes” which effect interface

•gate very high voltage, drain at high voltage

•0.6um process, 12V Vgs, 6V Vds with a 5V part

•high current needed

•tox control not as critical