EE461g: Introduction to Electronic Circuits

Lecture 2

Dr. Lau

University of Kentucky

Outline

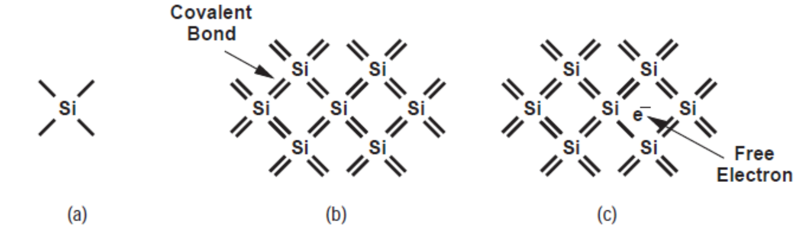


Figure 2.3 (a) Silicon atom, (b) covalent bonds between atoms, (c) free electron released by thermal energy.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

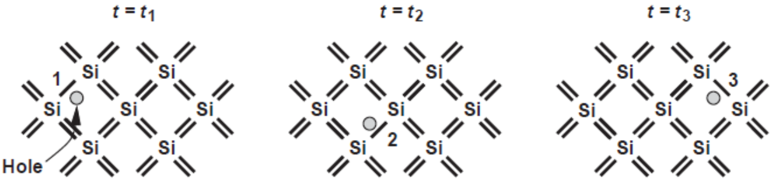


Figure 2.4 Movement of electron through crystal.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

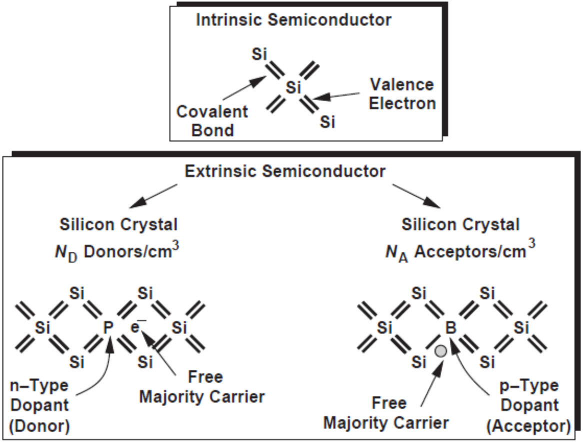


Figure 2.7 Summary of charge carriers in silicon.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

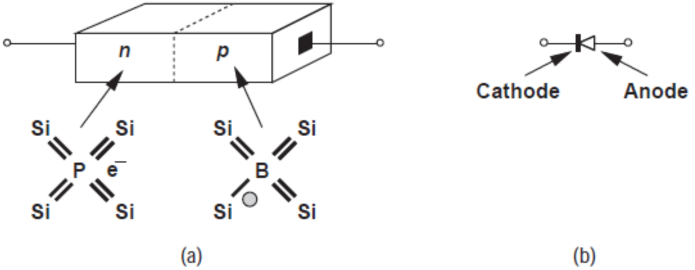


Figure 2.16 *pn* junction.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

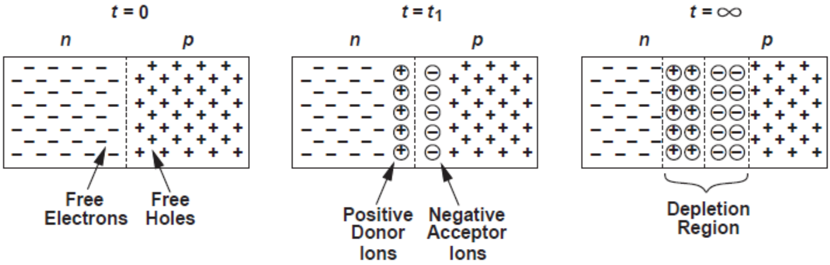


Figure 2.19 Evolution of charge concentrations in a *pn* junction.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

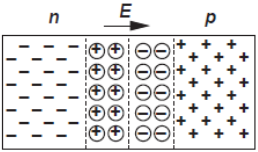


Figure 2.20 Electric field in a *pn* junction.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

Example 2.12

In the junction shown in Fig. 2.21, the depletion region has a width of b on the n side and a on the p side. Sketch the electric field as a function of x.

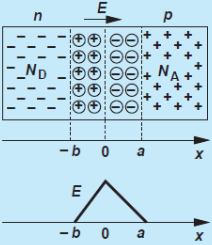


Figure 2.21 Electric field profile in a *pn* junction.

Solution Beginning at $x < -b$, we note that the absence of net charge yields $E = 0$. At $x > -b$, each positive donor ion contributes to the electric field, i.e., the magnitude of E rises as x approaches zero. As we pass $x = 0$, the negative acceptor atoms begin to contribute negatively to the field, i.e., E falls. At $x = a$, the negative and positive charge exactly cancel each other and $E = 0$.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

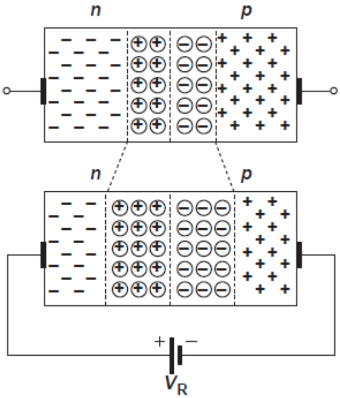


Figure 2.23 *pn* junction under reverse bias.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

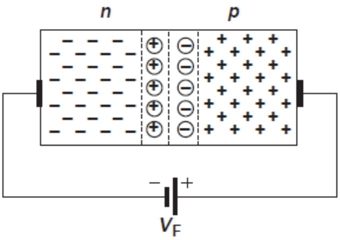


Figure 2.27 *pn* junction under forward bias.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

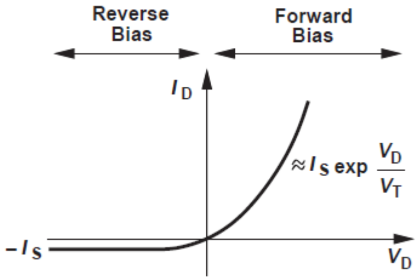


Figure 2.31 I/V characteristic of a *pn* junction.

Source: B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill, 2017.

PN Junction Diode: Current-Voltage Relationship

Shockley Diode Equation:

$$\boxed{I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)}$$

Parameters:

- I_D = diode current
- V_D = voltage across the diode
- I_S = reverse saturation current (typically 10^{-12} to 10^{-15} A)
- n = ideality factor (1 for ideal diode, 1–2 in practice)
- V_T = **thermal voltage** (see next slide)

Thermal Voltage

Definition:

$$\boxed{V_T = \frac{kT}{q}}$$

Constants:

- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = absolute temperature (Kelvin)
- q = electron charge = 1.6×10^{-19} C

At room temperature ($T = 300$ K): $\boxed{V_T \approx 26 \text{ mV}}$

SPICE Simulation: Diode I-V Characteristic

SPICE Netlist:

```
* Diode I-V Simulation

.model D1N4148 D(Is=1e-14
+  Rs=0.001 N=1.0)

Vin in 0 DC 0
D1 in 0 D1N4148

.dc Vin -1 5 0.001

.end
```

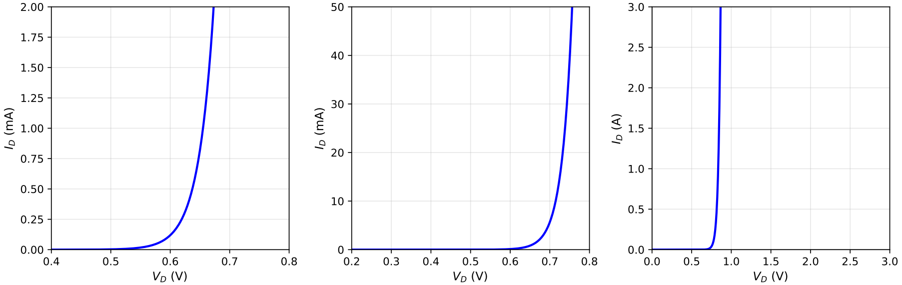
Parameters:

- $I_S = 10^{-14}$ A
- $n = 1.0$ (ideal)
- $R_S \approx 0$

DC Sweep:

- V_D from -1 to 5 V
- Step size: 1 mV

Diode I-V Characteristic: Effect of Scale



Piecewise Linear Diode Models

Goal: Analyze diode circuits using simplified models

We will use three **piecewise linear models** of increasing accuracy:

1. **Ideal Diode Model** — Switch closes at $V_D = 0$
2. **Constant Voltage Drop Model** — Switch closes at $V_D = V_f$
3. **Voltage Drop + Resistance Model** — Adds series resistance r_d

Each model approximates the exponential I_D–V_D curve with straight line segments.

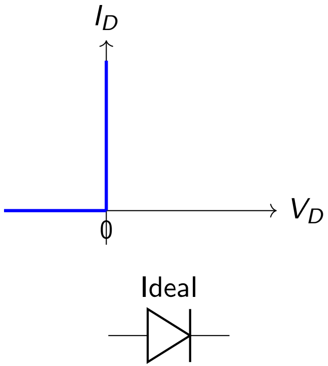
Behavior:

- Forward bias ($V_D \geq 0$): Short circuit
- Reverse bias ($V_D < 0$): Open circuit

Equations:

$$\text{If } V_D \geq 0: \quad V_D = 0, \; I_D \geq 0$$

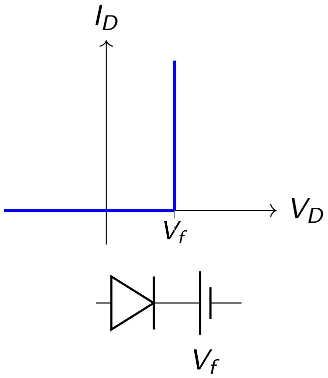
$$\text{If } V_D < 0: \quad I_D = 0$$



Model 2: Constant Voltage Drop

Behavior:

- Forward bias ($V_D \geq V_f$): $V_D = V_f$
- Reverse bias ($V_D < V_f$): Open circuit



Equations:

$$\text{If } V_D \geq V_f : \quad V_D = V_f, \; I_D \geq 0$$

$$\text{If } V_D < V_f : \quad I_D = 0$$

Typical: $V_f \approx 0.7$ V (silicon)

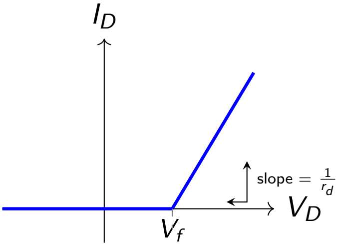
Model 3: Voltage Drop + Resistance

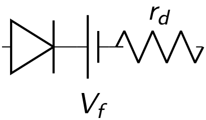
Behavior:

- Forward bias ($V_D \geq V_f$):

$$V_D = V_f + I_D \cdot r_d$$

- Reverse bias ($V_D < V_f$): Open circuit





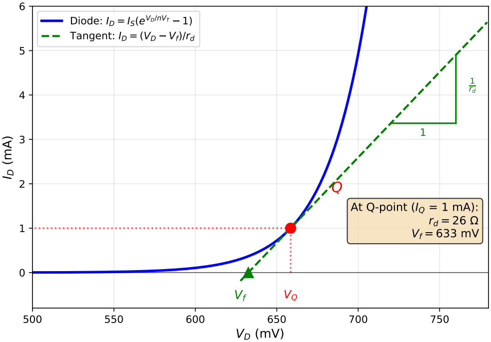
Equations:

$$\text{If } V_D \geq V_f : \quad I_D = \frac{V_D - V_f}{r_d}$$

$$\text{If } V_D < V_f : \quad I_D = 0$$

Deriving Model 3 from the Diode Equation

Goal: Find r_d and V_f by linearizing at a Q-point (V_Q, I_Q)



Approach:

1. Choose operating point Q
2. Find tangent line slope $\rightarrow r_d$
3. Find x-intercept $\rightarrow V_f$

The tangent line approximates the exponential curve near Q.

Deriving r_d: Small Signal Resistance

Start with Shockley equation:

$$I_D = I_S \left(e^{V_D/(nV_T)} - 1 \right) \approx I_S \, e^{V_D/(nV_T)} \quad \text{(forward bias)}$$

Take the derivative:

$$\frac{dI_D}{dV_D} = \frac{I_S}{nV_T} \, e^{V_D/(nV_T)} = \frac{I_D}{nV_T}$$

At Q-point, the slope is $1/r_d$:

$$\frac{1}{r_d} = \left. \frac{dI_D}{dV_D} \right|_Q = \frac{I_Q}{nV_T}$$

Small Signal Resistance

Result

$$\boxed{r_d = \frac{nV_T}{I_Q}}$$

For $n = 1$ and $V_T = 26$ mV:

$$r_d = \frac{26 \text{ mV}}{I_Q}$$

Examples:

- $I_Q = 1$ mA $\Rightarrow r_d = 26\ \Omega$
- $I_Q = 10$ mA $\Rightarrow r_d = 2.6\ \Omega$
- $I_Q = 0.1$ mA $\Rightarrow r_d = 260\ \Omega$

Deriving V_f: Forward Voltage

Tangent line equation at (V_Q, I_Q) with slope $1/r_d$:

$$I_D - I_Q = \frac{1}{r_d}(V_D - V_Q)$$

Find x-intercept (set $I_D = 0$):

$$0 - I_Q = \frac{1}{r_d}(V_f - V_Q)$$

$$V_f = V_Q - I_Q \cdot r_d = V_Q - I_Q \cdot \frac{nV_T}{I_Q}$$

Forward Voltage

Result

$$\boxed{V_f = V_Q - nV_T}$$

For $n = 1$ and $V_T = 26$ mV:

$$V_f = V_Q - 26 \text{ mV}$$

Example: At $I_Q = 1$ mA:

- $V_Q = nV_T \ln(I_Q/I_S) = 26 \text{ mV} \times \ln(10^{-3}/10^{-14}) \approx 659 \text{ mV}$
- $V_f = 659 - 26 = 633$ mV

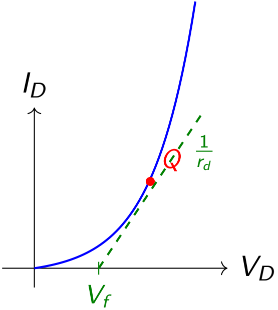
Summary: Piecewise Linear Model Parameters

Given a diode operating at Q-point (V_Q, I_Q):

Model 3 parameters:

$$r_d = \frac{nV_T}{I_Q}$$

$$V_f = V_Q - nV_T$$



For $n = 1$**:**

- $r_d = \dfrac{26 \text{ mV}}{I_Q}$
- $V_f = V_Q - 26 \text{ mV}$

Key insight: The model parameters depend on the operating point!

Verification: Measured vs. Theoretical Parameters

Method: Evaluate I_D at V_Q and $V_Q + 1\ \mu$V, fit line to find slope and x-intercept

Diode: $I_S = 10^{-14}$ A, $n = 1$, $V_T = 26$ mV

I_Q	V_Q	r_d (Theory)	r_d (Meas.)	V_f (Theory)	V_f (Meas.)
0.1 mA	598.7 mV	260.00 Ω	260.00 Ω	572.7 mV	572.7 mV
1 mA	658.5 mV	26.00 Ω	26.00 Ω	632.5 mV	632.5 mV
10 mA	718.4 mV	2.60 Ω	2.60 Ω	692.4 mV	692.4 mV

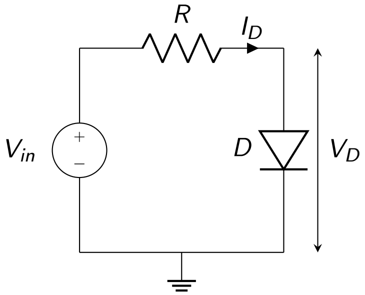
Key results:

- Measured slope $= 1/r_d$ matches $I_Q/(nV_T)$ within 0.002%
- Measured x-intercept $= V_f$ matches $V_Q - nV_T$ within 0.0001%
- Formulas are **exact** for the exponential diode model

Example: Analyzing a Diode Circuit

Goal: Apply the ideal diode model (Model 1) using the proof by contradiction method

Circuit:



Given:

- $R = 100\ \Omega$
- Ideal diode (Model 1)

Find: V_D and I_D as functions of V_{in}

Ideal Diode:

$$\text{ON: } V_D = 0,\ \ I_D \geq 0$$

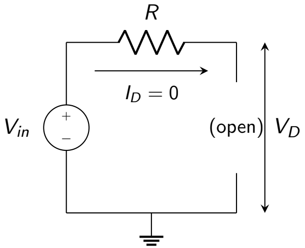
$$\text{OFF: } I_D = 0,\ \ V_D < 0$$

SPICE Netlist

```
* Diode Circuit - Model 1

Vin in 0 DC 0
R1 in diode 100

* Near-ideal diode
.model DIDEAL D(Is=1e-14 N=1 Rs=0.001)
D1 diode 0 DIDEAL

.dc Vin -5 10 0.01
.print dc V(diode) I(D1)
.end
```

Assumption: $V_D < 0$, so $I_D = 0$

Replace diode with open circuit:



Analysis with $I_D = 0$:

- No current through R
- No voltage drop across R
- Therefore: $V_D = V_{in}$

$$\boxed{V_D = V_{in}, \quad I_D = 0}$$

Test Guess #1: Check for Contradiction

Our guess assumed: $V_D < 0$
Our solution gave: $V_D = V_{in}$

Test: When is $V_D \geq 0$? (contradiction!)

$$V_{in} \geq 0 \quad \Rightarrow \quad V_D \geq 0$$

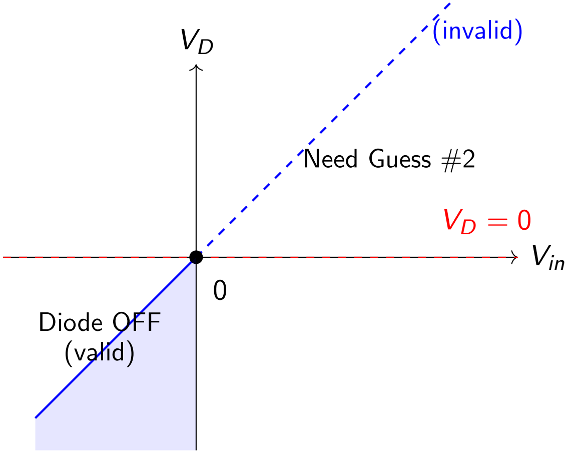
Contradiction Found!

For $V_{in} \geq 0$, our solution gives $V_D \geq 0$,
but we assumed $V_D < 0$ (diode OFF).

$\Rightarrow$ Our guess is **wrong** in this region!

Conclusion: Guess #1 is only valid for $V_{in} < 0$

Guess #1: Valid Region



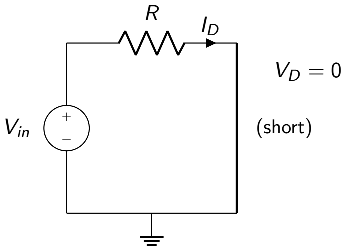
For $V_{in} < 0$: Diode is OFF

$$V_D = V_{in}, \quad I_D = 0 \quad \checkmark$$

Guess #2: Diode is ON ($V_D = 0$)

For $V_{in} \geq 0$: Try the other state

Assumption: $V_D = 0$, so diode is a short circuit



Analysis with $V_D = 0$:
Apply KVL:

$$V_{in} = I_D \cdot R + V_D = I_D \cdot R + 0$$

$$I_D = \frac{V_{in}}{R}$$

$$\boxed{V_D = 0, \quad I_D = \frac{V_{in}}{R}}$$

Test Guess #2: Verify Consistency

Our guess assumed: $I_D \geq 0$ (current flows through diode)

Our solution gave: $I_D = \dfrac{V_{in}}{R}$

Check: Is $I_D \geq 0$ when $V_{in} \geq 0$?

$$I_D = \frac{V_{in}}{R} \geq 0 \quad \text{when} \quad V_{in} \geq 0 \quad \checkmark$$

No Contradiction!

When $V_{in} \geq 0$, we get $I_D \geq 0$.
This is consistent with our guess (diode ON). ✓

Complete Solution: V_D and I_D vs V_{in}

Region 1: $V_{in} < 0$ (Diode OFF)

$$V_D = V_{in}, \qquad I_D = 0$$

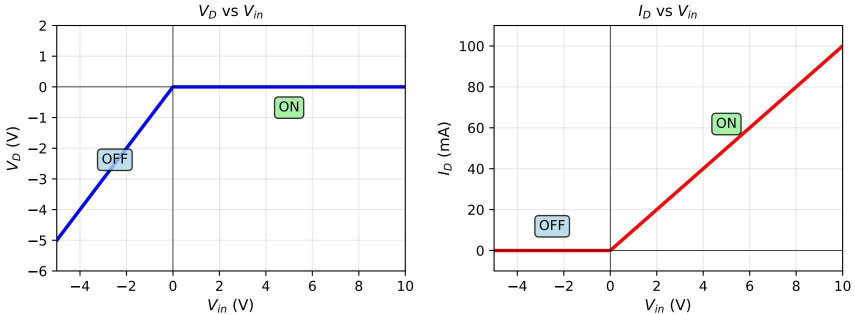
Region 2: $V_{in} \geq 0$ (Diode ON)

$$V_D = 0, \qquad I_D = \frac{V_{in}}{R}$$

Key observations:

- Transition occurs at $V_{in} = 0$
- When OFF: diode blocks current, voltage follows input
- When ON: diode conducts, voltage clamped to zero

Graphical Solution (Model 1)



With $R = 100\ \Omega$**:** At $V_{in} = 10$ V, $I_D = 100$ mA

Model 2 Analysis: Same Circuit

Using Model 2 (Constant Voltage Drop, $V_f = 0.7$ V):

Region 1: $V_{in} < V_f$ (Diode OFF)

$$V_D = V_{in}, \qquad I_D = 0$$

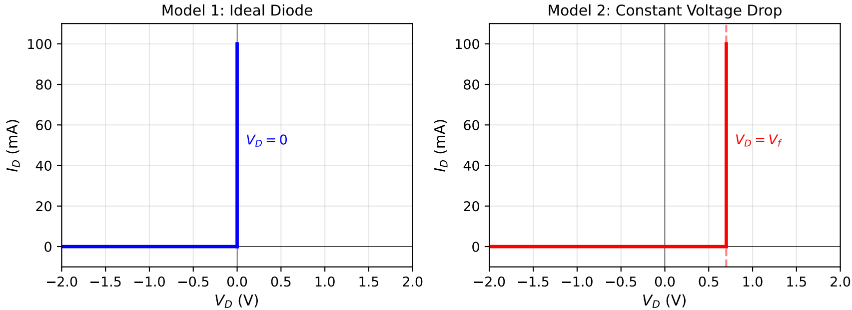
Region 2: $V_{in} \geq V_f$ (Diode ON)

$$V_D = V_f, \qquad I_D = \frac{V_{in} - V_f}{R}$$

Comparison to Model 1:

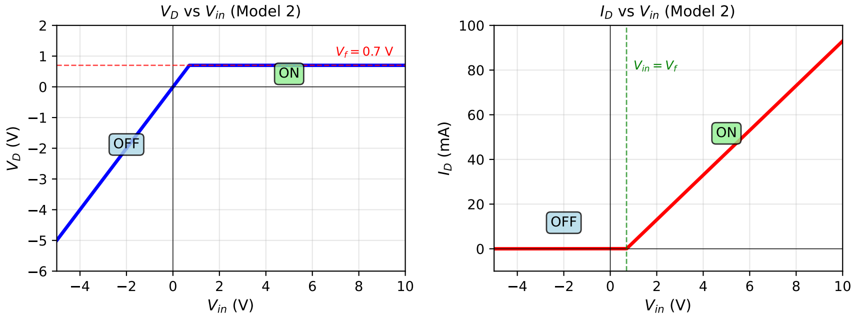
- Transition now at $V_{in} = V_f = 0.7$ V (not 0 V)
- When ON: V_D clamps to V_f (not 0 V)
- Current is reduced by the V_f drop

Model 1 vs Model 2: I-V Characteristics



Key difference: Model 2 turns ON at $V_D = V_f$ instead of $V_D = 0$

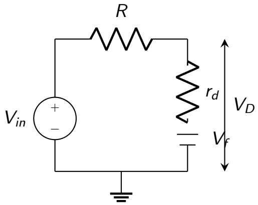
Graphical Solution (Model 2)



With $R = 100\ \Omega$**,** $V_f = 0.7$ **V:** At $V_{in} = 10$ V, $I_D = 93$ mA

Model 3 Analysis: Same Circuit

Using Model 3 ($V_f = 0.7$ V, $r_d = 2.6\ \Omega$):



When ON ($V_{in} \geq V_f$):
Apply KVL:

$$V_{in} = I_D \cdot R + V_D$$

$$V_D = V_f + I_D \cdot r_d$$

Solving:

$$I_D = \frac{V_{in} - V_f}{R + r_d}$$

$$V_D = V_f + \frac{r_d}{R + r_d}(V_{in} - V_f)$$

Model 3: Small Slope in V_D

Complete Solution

OFF ($V_{in} < V_f$): $V_D = V_{in}$, $I_D = 0$

ON ($V_{in} \geq V_f$):

$$V_D = V_f + \frac{r_d}{R + r_d}(V_{in} - V_f)$$

Key observation: When ON, V_D has a small positive slope:

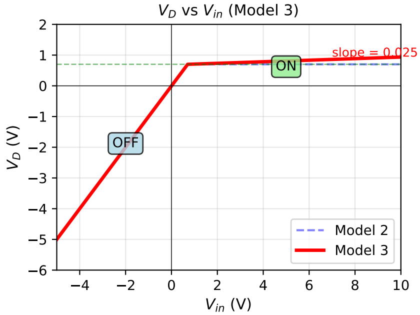
$$\frac{dV_D}{dV_{in}} = \frac{r_d}{R + r_d}$$

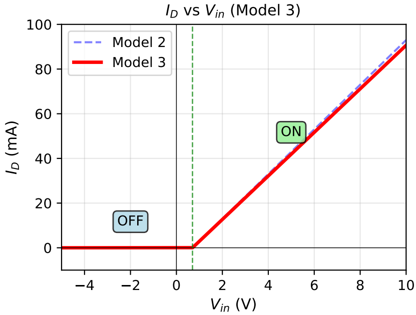
Example: With $R = 100\ \Omega$, $r_d = 2.6\ \Omega$:

$$\text{slope} = \frac{2.6}{100 + 2.6} = 0.025$$

Instead of V_D being flat at V_f, it rises slightly with V_{in}!

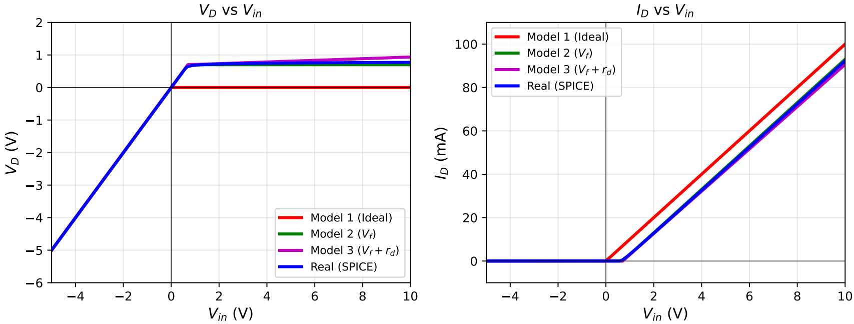
Graphical Solution (Model 3)





Note the small slope in V_D when ON (exaggerated here for visibility)

Comparison: All Three Piecewise Linear Models



Parameters: $R = 100\ \Omega,\ V_f = 0.7\ \text{V},\ r_d = 2.6\ \Omega$

Summary: Piecewise Linear Diode Models

We have three piecewise linear models of increasing accuracy:

1. **Model 1 (Ideal Diode):** $V_D = 0$ when ON
   - Simplest model — diode is a switch
   - Use when $V_f \ll$ other voltages in circuit
2. **Model 2 (Constant Voltage Drop):** $V_D = V_f$ when ON
   - Accounts for forward voltage drop ($V_f \approx 0.7$ V for Si)
   - Use for most hand calculations
3. **Model 3 (Voltage Drop + Resistance):** $V_D = V_f + I_D r_d$ when ON
   - Adds small-signal resistance $r_d = nV_T / I_Q$
   - Most accurate — use for detailed analysis near Q-point

Key insight: Choose model complexity based on required accuracy!