EE461g: Introduction to Electronic Circuits

Lecture 8

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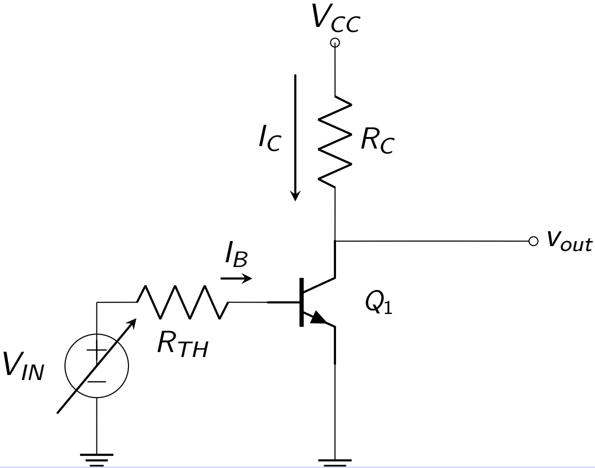
Outline

1. The Circuit
2. Designing the Q-Point
3. Edge of Saturation
4. Effect of R_C
5. Parallel CE Amplifiers
6. What If $R_{C1} \neq R_{C2}$?
7. Adding a Base Resistor
8. Merging to a Single R_C
9. Diode-Connected BJT
10. Active Load

The Circuit

CE Amplifier with Thévenin Source Resistance



Key change: $V_{BE} \neq V_{IN}$ — some voltage drops across R_{TH}

Circuit parameters: $V_{CC} = 10$ V, $R_C = 100\ \Omega$, $R_{TH} = 100\ \Omega$, $\beta = 100$, $I_S = 10^{-14}$ A

Designing the Q-Point

The Problem

We know that $V_{out} = V_{CE}$ can range between:

$$V_{CE,sat} \ \leq \ V_{CE} \ \leq \ V_{CC}$$

For **maximum symmetric swing**, we want the Q-point midway:

$$V_{CE,Q} = \frac{V_{CC} + V_{CE,sat}}{2} \approx \frac{10 + 0.2}{2} \approx 5 \text{ V}$$

This requires:

$$I_C = \frac{V_{CC} - V_{CE,Q}}{R_C} = \frac{10 - 5}{100} = 50 \text{ mA}$$

Question: What value of V_{IN} do we need to achieve $I_C = 50$ mA?

Finding the Required V_{IN}

We need $I_C = 50$ mA. Work backwards through the circuit:

Step 1: Base current: $I_B = \frac{I_C}{\beta} = \frac{50 \text{ mA}}{100} = 0.5$ mA

Step 2: Base-emitter voltage (from $I_C = I_S\, e^{V_{BE}/V_T}$):

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = (26 \text{ mV}) \ln\left(\frac{50 \times 10^{-3}}{10^{-14}}\right) = (26 \text{ mV})(29.24) = 0.760 \text{ V}$$

Step 3: KVL:
$V_{IN} = V_{BE} + I_B \cdot R_{TH} = 0.760 + (0.5 \times 10^{-3})(100) = 0.760 + 0.050$

$$\boxed{V_{IN} = 0.810 \text{ V}}$$

Edge of Saturation

Edge of Saturation

At the **edge of saturation**, the transistor has:

$$V_{CE} = V_{CE,sat} = 0.2 \text{ V}$$

This is the **maximum collector current** the load line allows:

$$I_{C,max} = \frac{V_{CC} - V_{CE,sat}}{R_C} = \frac{10 - 0.2}{100} = 98 \text{ mA}$$

Any further increase in V_{IN} drives the transistor deeper into saturation, where I_C is no longer controlled by I_B.

Question: What value of V_{IN} puts us right at this edge?

Finding V_{IN} at the Edge of Saturation

We need $I_C = 98$ mA (the load-line limit). Same procedure as before:

Step 1: Base current: $I_B = \dfrac{I_C}{\beta} = \dfrac{98 \text{ mA}}{100} = 0.98 \text{ mA}$

Step 2: Base-emitter voltage (from $I_C = I_S\, e^{V_{BE}/V_T}$):

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = (26 \text{ mV}) \ln\left(\frac{98 \times 10^{-3}}{10^{-14}}\right) = (26 \text{ mV})(29.91) = 0.778 \text{ V}$$

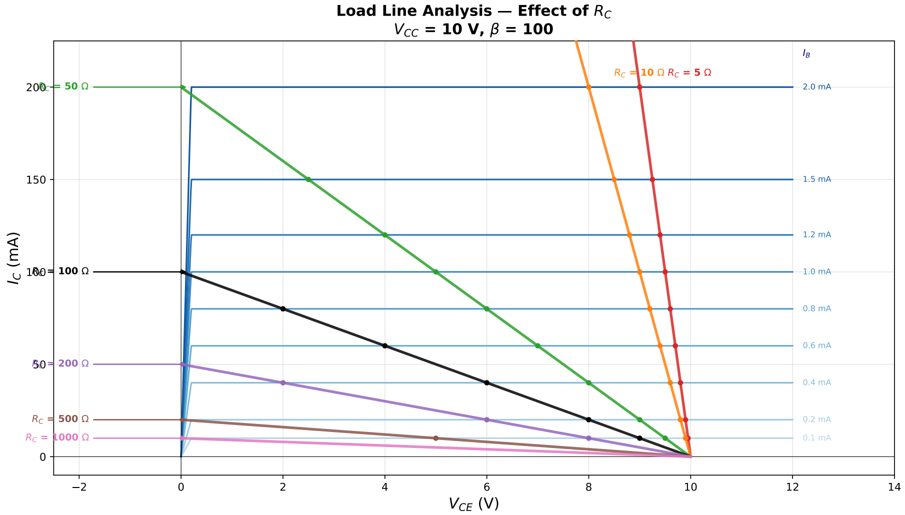
Step 3: KVL:
$V_{IN} = V_{BE} + I_B \cdot R_{TH} = 0.778 + (0.98 \times 10^{-3})(100) = 0.778 + 0.098$

$$\boxed{V_{IN} = 0.876 \text{ V}} \quad \text{(edge of saturation)}$$

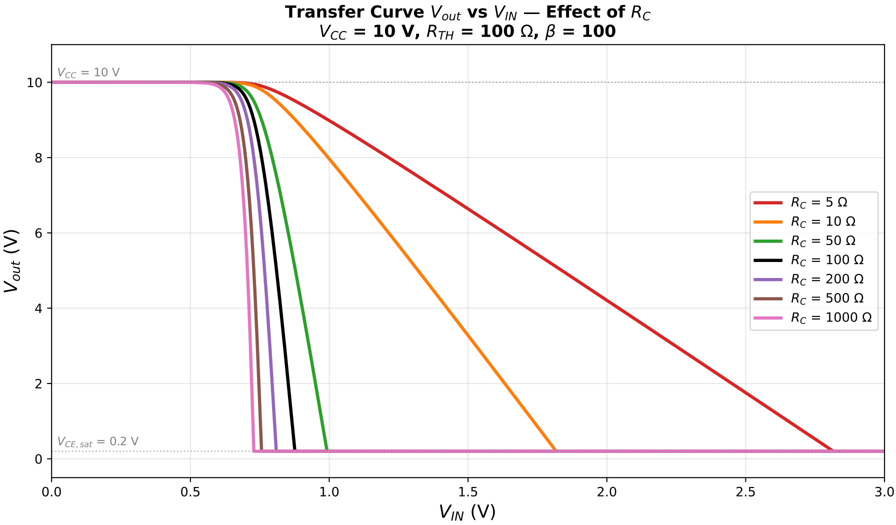
For $V_{IN} > 0.876$ V, the transistor saturates and $V_{out} \approx V_{CE,sat}$.

Effect of R_C

Effect of R_C on the Load Line



Transfer Curve V_{out} vs V_{IN} for Different R_C



Voltage Gain at $V_{out} = 6$ V

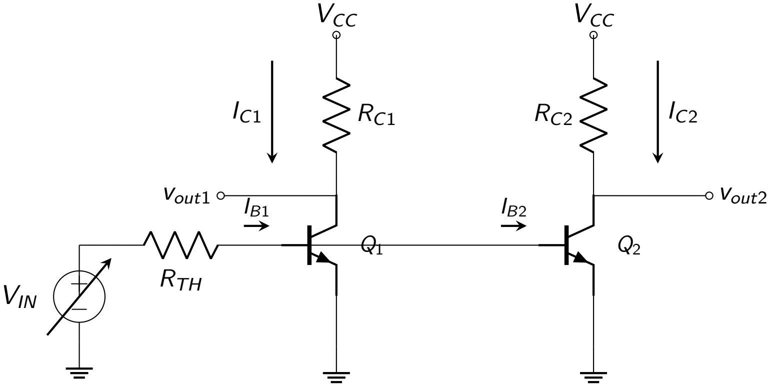
The slope of the transfer curve is the **large-signal voltage gain**:

$$\frac{dV_{out}}{dV_{IN}} = \frac{-\,I_C\,R_C\,/\,V_T}{1 + I_C\,R_{TH}\,/\,(\beta\,V_T)} \quad \text{where} \quad I_C = \frac{V_{CC} - V_{out}}{R_C} = \frac{4}{R_C}$$

R_C (Ω)	I_C (mA)	V_{IN} (V)	dV_{out}/dV_{IN}
5	800.0	1.632	−4.8
10	400.0	1.214	−9.4
50	80.0	0.852	−37.7
100	**40.0**	**0.794**	**−60.6**
200	20.0	0.756	−87.0
500	8.0	0.721	−117.6
1000	4.0	0.699	−133.3

Trade-off: Larger R_C gives higher gain, but requires smaller I_C and leaves less room before saturation.

Parallel CE Amplifiers



Same parameters: $V_{CC} = 10$ V, $R_{C1} = R_{C2} = 100\ \Omega$, $R_{TH} = 100\ \Omega$,
$\beta = 100$, $I_S = 10^{-14}$ A

Still using $V_{IN} = 0.810$ V (our single-BJT design)

KVL with Two Base Currents

R_{TH} now carries **both** base currents. KVL around the input loop:

$$\boxed{V_{IN} = V_{BE} + (I_{B1} + I_{B2}) \cdot R_{TH}}$$

Since both transistors are **identical** and share the same V_{BE}:

$$I_{B1} = I_{B2} \quad \Rightarrow \quad V_{IN} = V_{BE} + 2\, I_{B1} \cdot R_{TH}$$

Compare with the single-BJT case:

$$V_{IN} = V_{BE} + I_B \cdot R_{TH} \quad \text{(single)}$$

More current through R_{TH} $\Rightarrow$ larger voltage drop $\Rightarrow$ V_{BE} must decrease.

Solving for the New Operating Point

With $V_{IN} = 0.810$ V and two identical BJTs:

$$0.810 = V_{BE} + 2 \cdot \frac{I_S\, e^{V_{BE}/V_T}}{\beta} \cdot R_{TH}$$

Solving numerically (with $V_T = 26$ mV):

	Single BJT	**Parallel BJTs (each)**
V_{BE}	0.760 V	0.748 V
I_B / I_{B1}	0.501 mA	0.311 mA
I_C / I_{C1}	50.1 mA	31.1 mA
V_{CE} / V_{CE1}	4.99 V	6.88 V
R_{TH} drop	50.1 mV	$2 \times 31.1 = 62.2$ mV

I_{B1} and I_{B2} are each **38% smaller** than the single-BJT I_B, and V_{CE} shifted from 4.99 V to 6.88 V.

Both Q-points have moved **toward cutoff**!

Textbook Method: Iterative Solution

The textbook solves $V_{IN} = V_{BE} + 2\,I_{B1} \cdot R_{TH}$ by repeated substitution:

1. Guess V_{BE}
2. $I_{B1} = (V_{IN} - V_{BE})\,/\,(2\,R_{TH}), \quad I_{C1} = \beta\,I_{B1}$
3. New $V_{BE} = V_T \ln(I_{C1}/I_S)$
4. Repeat until converged

Starting with $V_{BE} = 0.7$ V:

Iter	V_{BE} (V)	I_{B1} (mA)	I_{C1} (mA)	$V_{BE,new}$ (V)
1	0.7000	0.550	55.00	0.7627
2	0.7627	0.236	23.64	0.7408
3	0.7408	0.346	34.61	0.7507
4	0.7507	0.297	29.65	0.7467
5	0.7467	0.317	31.67	0.7484
6	0.7484	0.308	30.81	0.7477
7	0.7477	0.312	31.17	0.7480
8	0.7480	0.310	31.02	0.7478
9	0.7478	0.311	31.08	**0.7479**

Converges to $V_{BE} = 0.748$ V, $I_{B1} = 0.311$ mA, $I_{C1} = 31.1$ mA — matches our result.

SPICE Simulation — Single CE Amplifier

```
* Single CE Amplifier - Operating Point
Vcc vcc 0 DC 10
Vin in 0 DC 0.810
Rth in base 100
Q1 collector base 0 IDEALNJT
Rc vcc collector 100
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

SPICE operating-point results:

V_{BE}	0.760 V
I_B	0.501 mA
I_C	50.1 mA
V_{CE}	4.99 V

Note: TEMP=TNOM=28.42°C so that $V_T = kT/q = 26.0$ mV

SPICE Simulation — Parallel CE Amplifiers

```
* Parallel CE Amplifiers - Operating Point
Vcc1 vcc1 0 DC 10
Vcc2 vcc2 0 DC 10
Vin in 0 DC 0.810
Rth in base 100
Q1 collector1 base 0 IDEALNJT
Q2 collector2 base 0 IDEALNJT
Rc1 vcc1 collector1 100
Rc2 vcc2 collector2 100
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

SPICE operating-point results (each transistor):

V_{BE}	0.748 V
$I_{B1} = I_{B2}$	0.312 mA
$I_{C1} = I_{C2}$	31.2 mA
$V_{CE1} = V_{CE2}$	6.88 V

Numerical vs. SPICE Results

	Single BJT		Parallel (each)	
	Numerical	SPICE	Numerical	SPICE
V_{BE}	0.760 V	0.760 V	0.748 V	0.748 V
I_B	0.501 mA	0.501 mA	0.312 mA	0.312 mA
I_C	50.1 mA	50.1 mA	31.2 mA	31.2 mA
V_{CE}	4.99 V	4.99 V	6.88 V	6.88 V

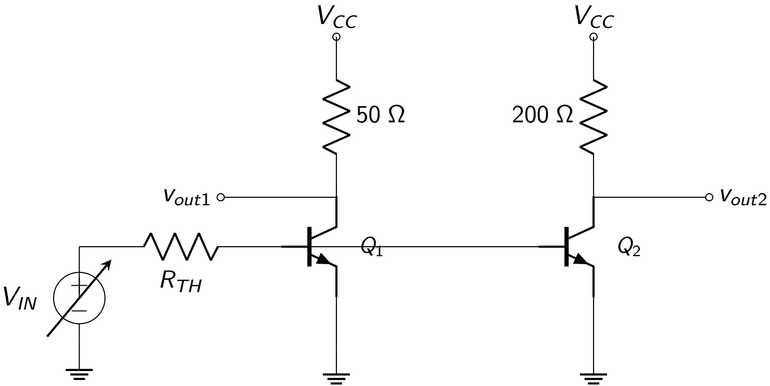
Numerical and SPICE results agree when the same V_T is used.

SPICE default is $T = 27\,^\circ\mathrm{C} \Rightarrow V_T = 25.86$ mV.

We set `TEMP = TNOM = 28.42°C` so $V_T = 26.0$ mV (matching our hand analysis).

What If $R_{C1} \neq R_{C2}$?

Parallel CE Amplifiers with Different R_C



Same transistors, same $V_{IN} = 0.810$ V, same $R_{TH} = 100\ \Omega$ — but $R_{C1} = 50\ \Omega$, $R_{C2} = 200\ \Omega$

SPICE Simulation — Different R_C Values

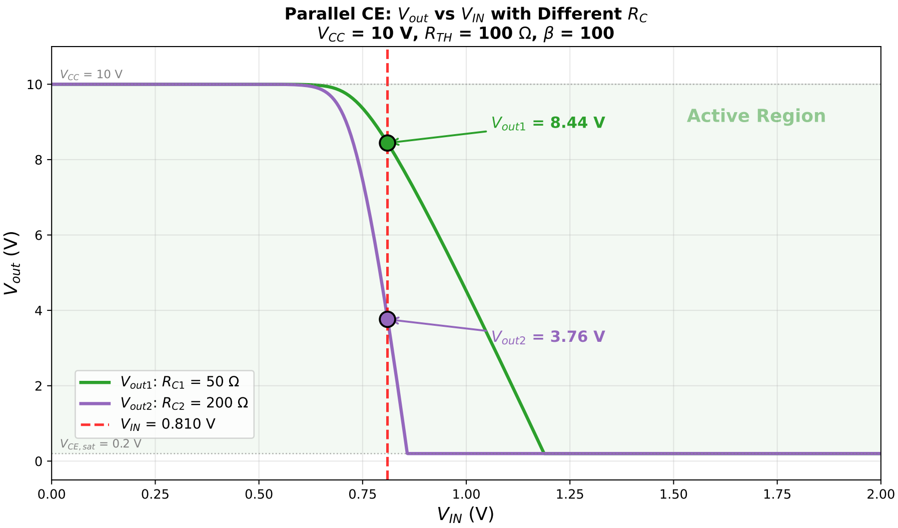
```
* Parallel CE - Different RC values
Vcc1 vcc1 0 DC 10
Vcc2 vcc2 0 DC 10
Vin in 0 DC 0.810
Rth in base 100
Q1 collector1 base 0 IDEALNJT
Q2 collector2 base 0 IDEALNJT
Rc1 vcc1 collector1 50
Rc2 vcc2 collector2 200
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

SPICE operating-point results:

	Q_1 ($R_{C1} = 50\ \Omega$)	Q_2 ($R_{C2} = 200\ \Omega$)
V_{BE}	0.748 V	0.748 V
I_B	0.312 mA	0.312 mA
I_C	31.2 mA	31.2 mA
V_{CE}	**8.44 V**	**3.76 V**

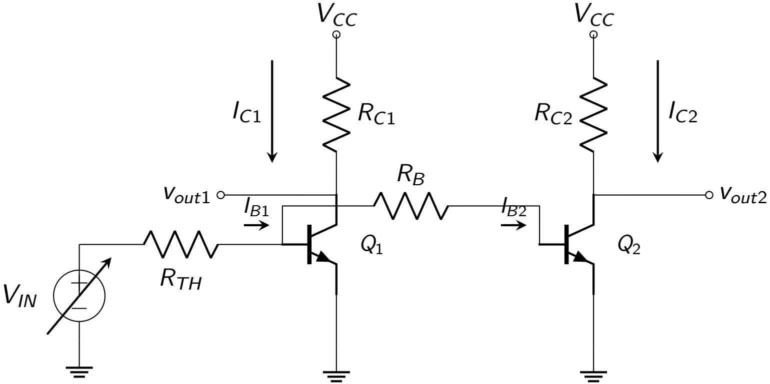
I_B and I_C are **identical** — they depend only on V_{BE}, not on R_C.
R_C only affects $V_{CE} = V_{CC} - I_C \cdot R_C$.

Transfer Curves: $R_{C1} = 50\ \Omega$ vs. $R_{C2} = 200\ \Omega$



Adding a Base Resistor

Parallel CE with Resistor Between Bases



$R_{C1} = R_{C2} = 100\ \Omega, \quad R_{TH} = 100\ \Omega, \quad R_B = 10\ \Omega, \quad V_{IN} = 0.810\ \text{V}$

SPICE Simulation — Base Resistor $R_B = 10\ \Omega$

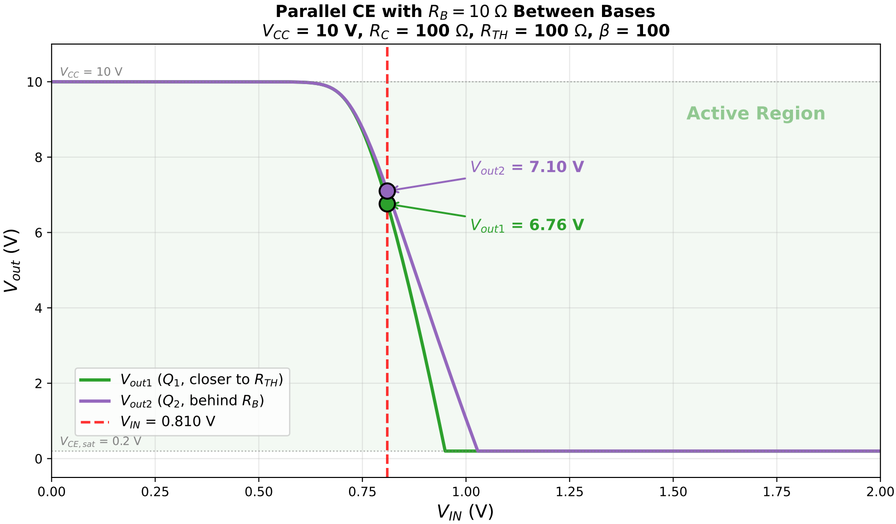
```
* Parallel CE with Base Resistor
Vcc1 vcc1 0 DC 10
Vcc2 vcc2 0 DC 10
Vin in 0 DC 0.810
Rth in base1 100
Rb base1 base2 10
Q1 collector1 base1 0 IDEALNJT
Q2 collector2 base2 0 IDEALNJT
Rc1 vcc1 collector1 100
Rc2 vcc2 collector2 100
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

SPICE operating-point results:

	Q_1	Q_2
V_{BE}	0.7486 V	0.7457 V
I_B	0.324 mA	0.290 mA
I_C	32.4 mA	29.0 mA
V_{CE}	6.76 V	7.10 V

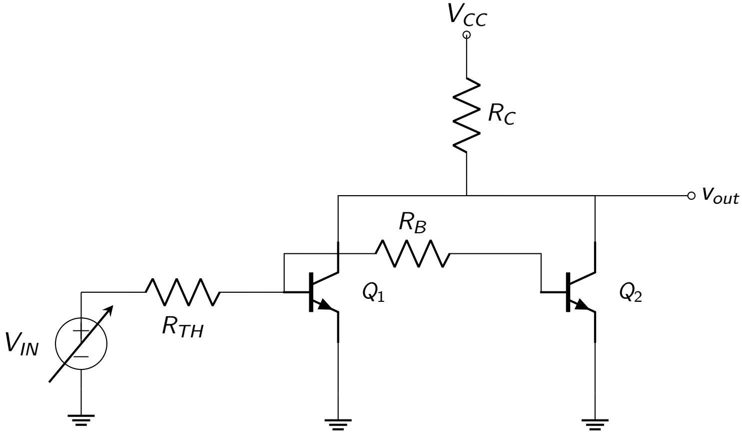
R_B drops only $I_{B2} \times R_B = 2.9$ mV, but this causes I_{C1} and I_{C2} to differ by **12%**.

Transfer Curves with $R_B = 10\ \Omega$ Between Bases



Merging to a Single R_C

Parallel CE with Shared R_C



$$R_C = 100\ \Omega, \quad R_{TH} = 100\ \Omega, \quad R_B = 10\ \Omega, \quad V_{IN} = 0.810\ \text{V}$$

Now $I_C = I_{C1} + I_{C2}$ flows through a single R_C, and both transistors share the same V_{CE}.

SPICE Simulation — Shared R_C

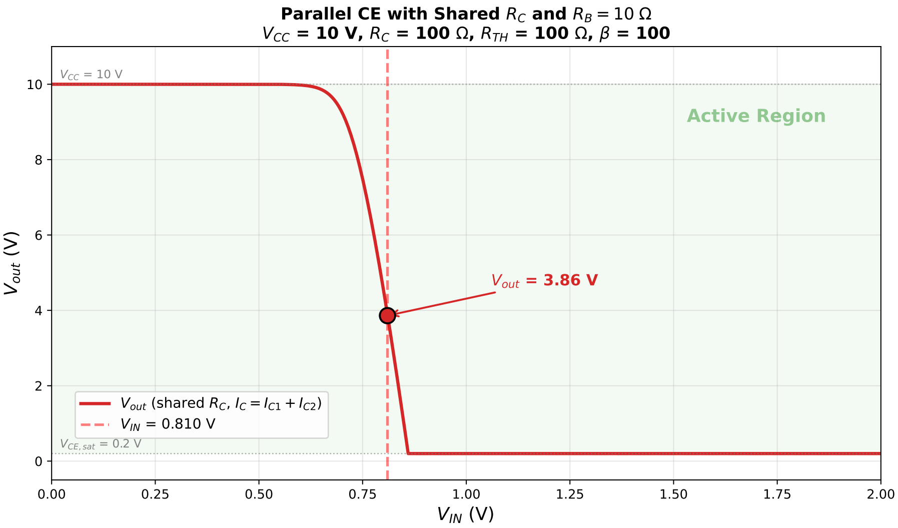
```
* Parallel CE - Base Resistor, Single RC
Vcc vcc 0 DC 10
Vin in 0 DC 0.810
Rth in base1 100
Rb base1 base2 10
Q1 collector base1 0 IDEALNJT
Q2 collector base2 0 IDEALNJT
Rc vcc collector 100
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

SPICE operating-point results:

	Q_1	Q_2
V_{BE}	0.7486 V	0.7457 V
I_B	0.324 mA	0.290 mA
I_{C1}, I_{C2}	32.4 mA	29.0 mA
$I_{C,total} = I_{C1} + I_{C2} = 61.4$ mA		$V_{CE} = V_{out} = 3.86$ V

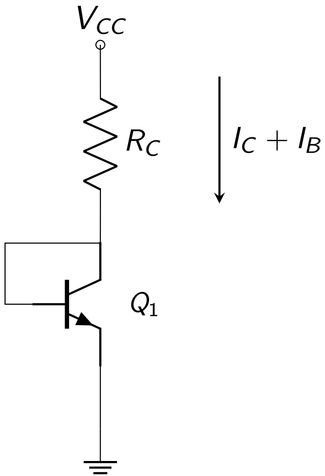
I_B and I_C for each transistor are **unchanged** from the two-R_C case.
Merging R_C only changes V_{CE}.

Transfer Curve: Shared R_C with $R_B = 10\ \Omega$



Diode-Connected BJT

Diode-Connected BJT



Base tied to collector $\Rightarrow$ $V_B = V_C$ $\Rightarrow$ $V_{BE} = V_{CE}$

The transistor acts like a **diode**: current $I_C + I_B$ flows through R_C.

$V_{CC} = 10$ V, $R_C = 100\ \Omega$, $\beta = 100$, $I_S = 10^{-14}$ A

Setting Up the Equations

Since $V_B = V_C$ and $V_E = 0$:

$$V_{BE} = V_{CE} = V_C$$

KCL at the collector/base node:

$$\frac{V_{CC} - V_C}{R_C} = I_C + I_B = I_C\left(1 + \frac{1}{\beta}\right) = I_E$$

Combined with $I_C = I_S\, e^{V_{BE}/V_T}$:

$$\boxed{\frac{V_{CC} - V_{BE}}{R_C} = I_S\, e^{V_{BE}/V_T}\left(1 + \frac{1}{\beta}\right)}$$

One equation, one unknown (V_{BE}) — solve by iteration.

Solving by Iteration

Textbook method:

1. Guess V_{BE}
2. $I_E = (V_{CC} - V_{BE})\,/\,R_C, \quad I_C = I_E \cdot \beta/(\beta+1), \quad I_B = I_E/(\beta+1)$
3. New $V_{BE} = V_T \ln(I_C/I_S)$
4. Repeat until converged

Starting with $V_{BE} = 0.7$ V:

Iter	V_{BE} (V)	I_E (mA)	I_C (mA)	I_B (mA)	$V_{BE,new}$ (V)
1	0.7000	93.00	92.08	0.921	0.7761
2	0.7761	92.24	91.33	0.913	**0.7759**
3	0.7759	92.24	91.33	0.913	**0.7759**

Converged result:

$V_B = V_C = V_{BE} = V_{CE}$	0.776 V
V_E	0 V
I_C	91.3 mA
I_B	0.913 mA
$I_E = I_C + I_B$	92.2 mA

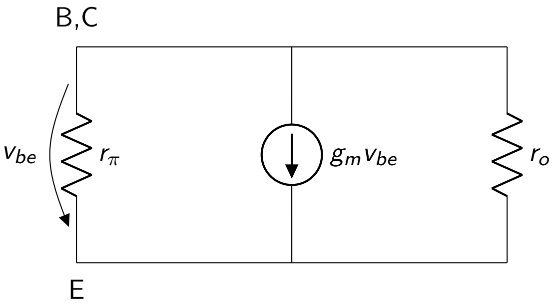
SPICE Verification

```
* Diode-Connected BJT (base tied to collector)
Vcc vcc 0 DC 10
Rc vcc collector 100
Q1 collector collector 0 IDEALNJT
.model IDEALNJT NPN(IS=1e-14 BF=100)
.options TEMP=28.42 TNOM=28.42
```

	Numerical	SPICE
$V_B = V_C = V_{BE} = V_{CE}$	0.776 V	0.776 V
V_E	0 V	0 V
I_C	91.3 mA	91.3 mA
I_B	0.913 mA	0.913 mA
$I_E = I_C + I_B$	92.2 mA	92.2 mA

Numerical and SPICE agree exactly (both using $V_T = 26.0$ mV).

Small-Signal Model: Diode-Connected BJT

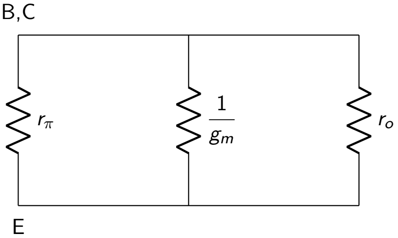


Since B and C are tied together, v_{be} appears across **all three** elements:

- r_π: current $= v_{be} \,/\, r_\pi$ (Ohm's law)
- $g_m v_{be}$: current $= g_m \cdot v_{be}$ (directly proportional to v_{be}!)
- r_o: current $= v_{be} \,/\, r_o$ (Ohm's law)

The dependent source $g_m v_{be}$ acts like a **resistor** $1/g_m$, because v_{be} is the voltage across it.

Replacing $g_m v_{be}$ with $1/g_m$



Three resistors in parallel — combine into one equivalent:

$$\boxed{r_{eq} = r_\pi \parallel \frac{1}{g_m} \parallel r_o}$$

With $I_C = 91.3$ mA, $\quad g_m = I_C/V_T = 3.51$ S, $\quad r_\pi = \beta/g_m = 28.5\ \Omega$, $\quad r_o \to \infty$:

$$r_{eq} = 28.5 \parallel 0.285 \parallel \infty = \frac{r_\pi}{1+\beta} = \frac{28.5}{101} = 0.282\ \Omega \approx \frac{1}{g_m}$$

For large β: $r_{eq} \approx 1/g_m = V_T/I_C$. The diode-connected BJT looks like a **small resistance** to ground.

!

Tying the base to the collector creates an

ACTIVE LOAD

Large signal: acts like a **non-linear** resistor

Small signal: acts **exactly** like a resistor $r_{eq} \approx 1/g_m$

What Determines I_S? (Razavi, Eq. 4.10)

From device physics, the saturation current is:

$$\boxed{I_S = \frac{A_E\, q\, D_n\, n_i^2}{N_B\, W_B}}$$

Symbol	Meaning	Controlled by
A_E	Emitter area	**IC designer** (mask layout)
q	Electron charge	Fundamental constant
D_n	Electron diffusion coeff.	Process (material)
n_i	Intrinsic carrier conc.	Process (material, temp.)
N_B	Base doping	Process (fabrication)
W_B	Base width	Process (diffusion depths)

A_E is the **only** parameter the circuit designer controls — just like W/L in a MOSFET.

Doubling A_E doubles I_S, which doubles I_C at the same V_{BE}.

From A_E to g_m to $1/g_m$

Step 1: I_S scales with emitter area: $I_S = \dfrac{A_E\, q\, D_n\, n_i^2}{N_B\, W_B} \propto A_E$

Step 2: Collector current depends on I_S: $I_C = I_S\, e^{V_{BE}/V_T} \propto A_E$

Step 3: Transconductance depends on I_C: $g_m = \dfrac{I_C}{V_T} \propto A_E$

Step 4: The active load resistance is:

$$\boxed{\frac{1}{g_m} = \frac{V_T}{I_C} = \frac{V_T}{I_S\, e^{V_{BE}/V_T}} \propto \frac{1}{A_E}}$$

Larger $A_E \Rightarrow$ larger $I_S \Rightarrow$ larger $I_C \Rightarrow$ larger $g_m \Rightarrow$ **smaller** $1/g_m$
Compare MOSFET: larger $W/L \Rightarrow$ larger $K_n \Rightarrow$ larger $g_m \Rightarrow$ smaller $1/g_m$