EE461g: Introduction to Electronic Circuits

Lecture 10

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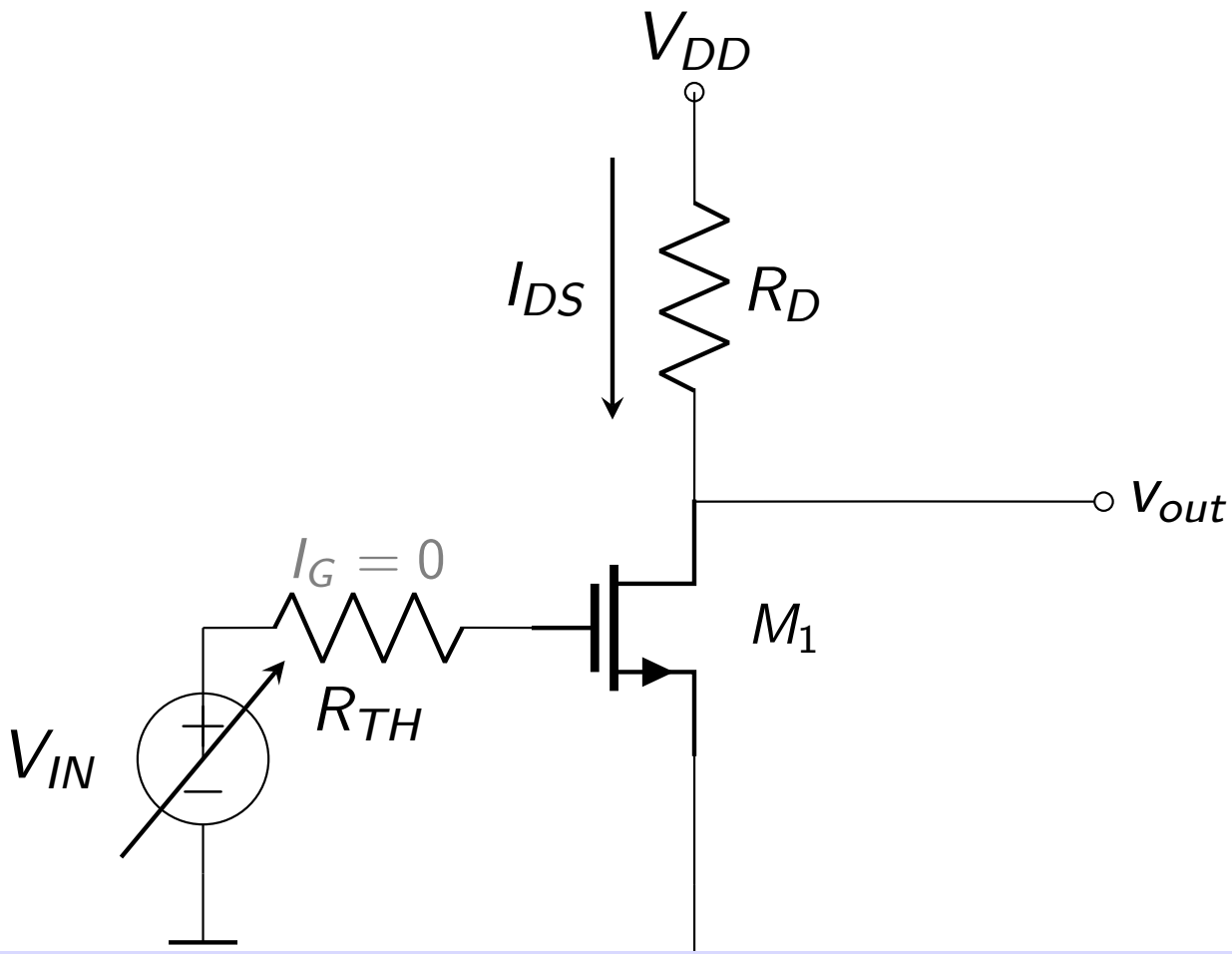
Outline

The Circuit

CS Amplifier with Thévenin Source Resistance



Key difference from BJT: $I_G = 0 \Rightarrow$ no voltage drop across $R_{TH} \Rightarrow V_{GS} = V_{IN}$

Circuit parameters: $V_{DD} = 10$ V, $R_D = 1$ kΩ, $R_{TH} = 100$ Ω, $K_n = 10$ mA/V^2, $V_{TN} = 0.7$ V

Designing the Q-Point

The Problem

We know that $V_{out} = V_{DS}$ can range between:

$$V_{GS} - V_{TN} \leq V_{DS} \leq V_{DD}$$

For **maximum symmetric swing**, we want the Q-point approximately midway:

$$V_{DS,Q} \approx \frac{V_{DD}}{2} = \frac{10}{2} = 5 \text{ V}$$

This requires:

$$I_{DS} = \frac{V_{DD} - V_{DS,Q}}{R_D} = \frac{10 - 5}{1000} = 5 \text{ mA}$$

Question: What value of V_{IN} do we need to achieve $I_{DS} = 5$ mA?

Finding the Required V_{IN}

We need $I_{DS} = 5$ mA. Since $I_G = 0$, we have $V_{GS} = V_{IN}$ directly:

Step 1: From $I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$:

$$V_{GS} - V_{TN} = \sqrt{\frac{2I_{DS}}{K_n}} = \sqrt{\frac{2 \times 5 \times 10^{-3}}{10 \times 10^{-3}}} = \sqrt{1} = 1.0 \text{ V}$$

Step 2: $V_{GS} = V_{TN} + 1.0 = 0.7 + 1.0 = 1.7$ V

Step 3: Since $I_G = 0$:

$$V_{IN} = V_{GS} + I_G \cdot R_{TH} = V_{GS} + 0 = V_{GS}$$

$$\boxed{V_{IN} = 1.700 \text{ V}}$$

No iteration needed! Unlike BJTs, we solve directly.
R_{TH} has **no effect** since $I_G = 0$.

Edge of Triode

Edge of Triode

At the **edge of triode**, the MOSFET satisfies:

$$V_{DS} = V_{GS} - V_{TN}$$

Unlike the BJT's fixed $V_{CE,sat} = 0.2$ V, this boundary **depends on** V_{GS}.

Combining with the load line $V_{DS} = V_{DD} - I_{DS} \cdot R_D$ and $I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$:
Let $x = V_{GS} - V_{TN}$:

$$x = V_{DD} - \frac{K_n}{2} x^2 R_D \quad \Rightarrow \quad \frac{K_n R_D}{2} x^2 + x - V_{DD} = 0$$

Question: What value of V_{IN} puts us right at this edge?

Finding V_{IN} at the Edge of Triode

With $\frac{K_n R_D}{2} = \frac{10 \times 10^{-3} \times 1000}{2} = 5$:

$$5x^2 + x - 10 = 0 \quad \Rightarrow \quad x = \frac{-1 + \sqrt{1 + 200}}{10} = \frac{-1 + \sqrt{201}}{10} = 1.318 \text{ V}$$

At the edge of triode:

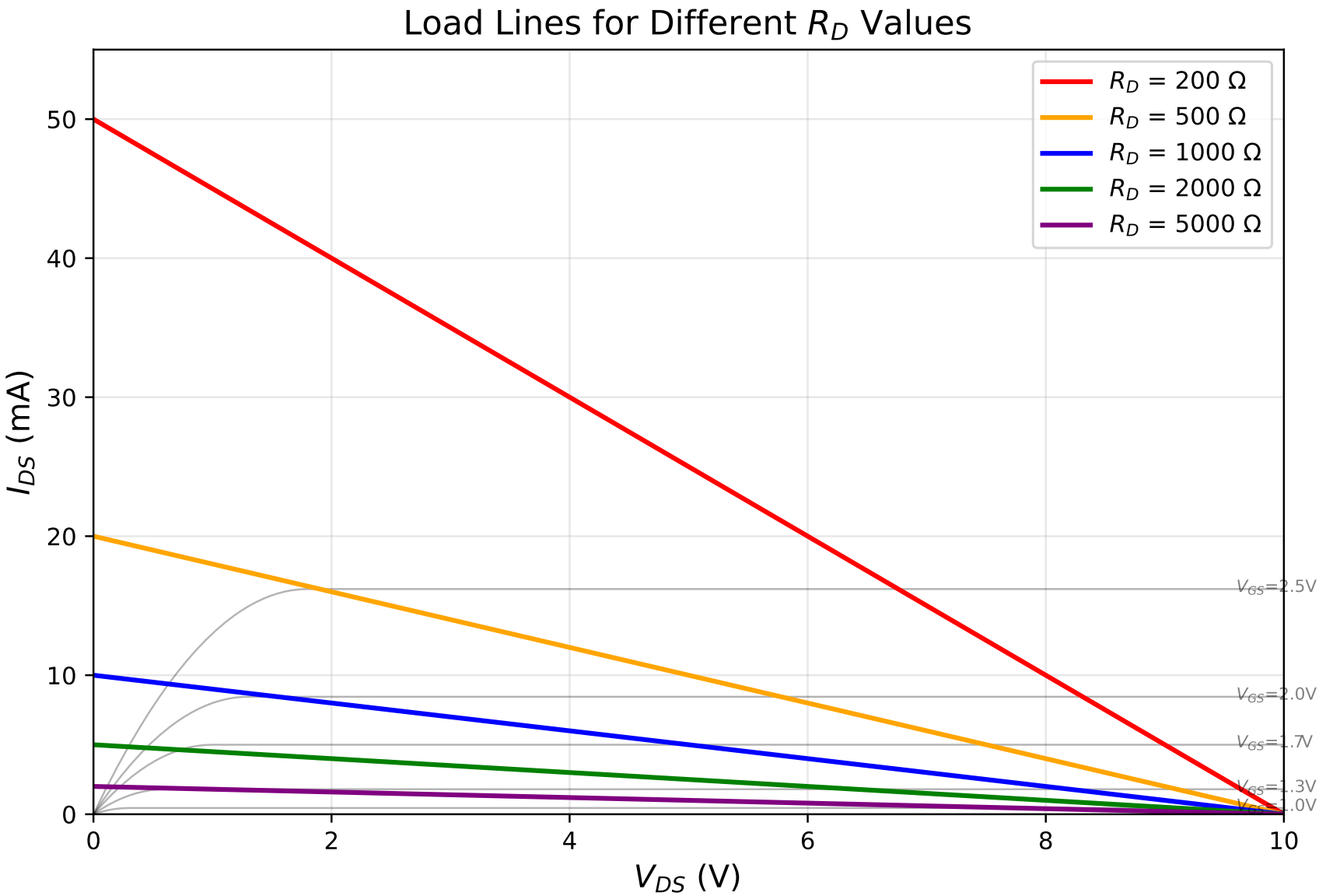
$V_{GS} = V_{IN}$	2.018 V
$V_{DS} = V_{GS} - V_{TN}$	1.318 V
I_{DS}	8.68 mA

$$\boxed{V_{IN} = 2.018 \text{ V}} \quad \text{(edge of triode)}$$

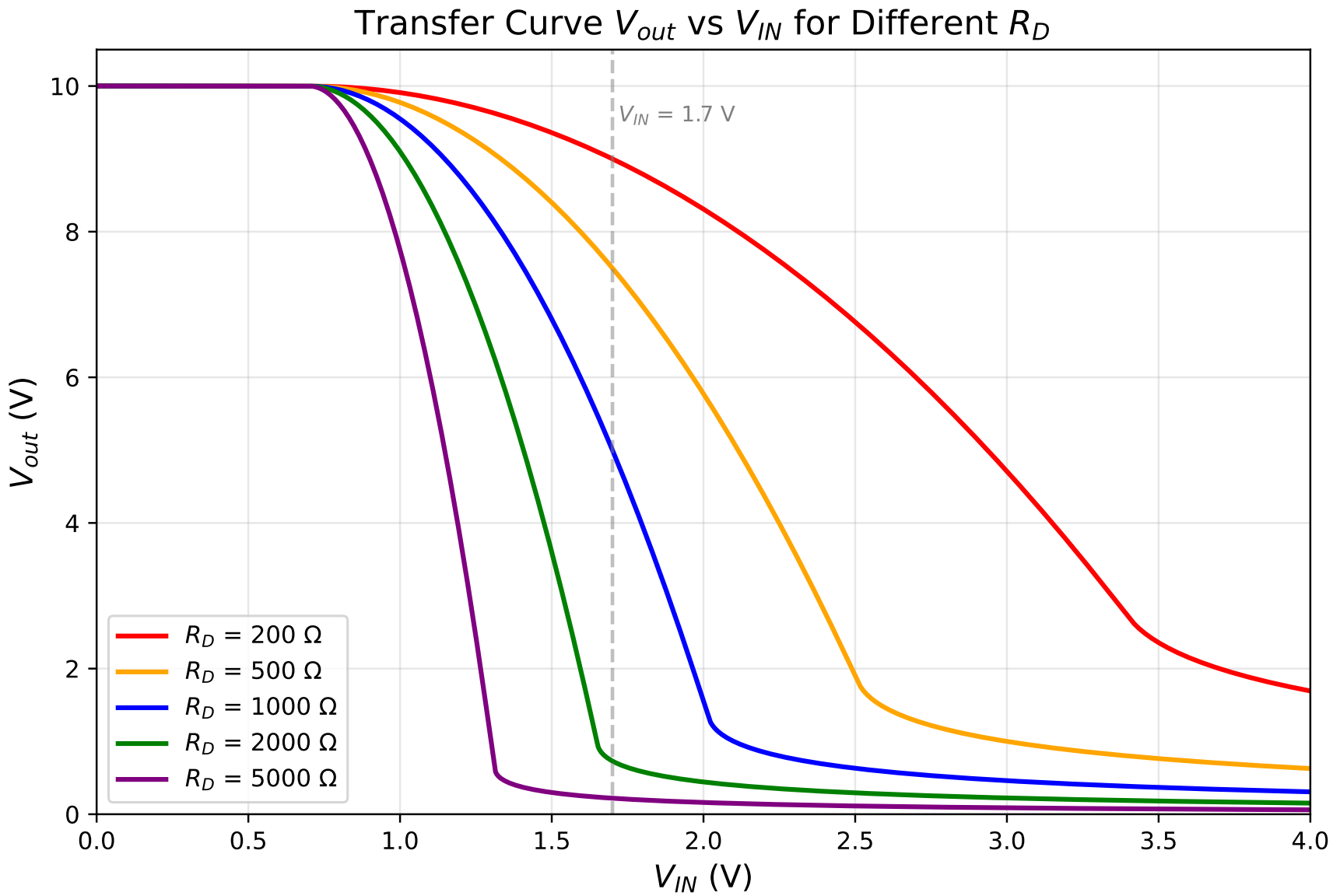
For $V_{IN} > 2.018$ V, the MOSFET enters the triode region.

Effect of R_D

Effect of R_D on the Load Line



Transfer Curve V_{out} vs V_{IN} for Different R_D



Voltage Gain at $V_{out} = 6$ V

The slope of the transfer curve (in saturation) is:

$$\frac{dV_{out}}{dV_{IN}} = -R_D \cdot g_m = -R_D \cdot K_n(V_{IN} - V_{TN})$$

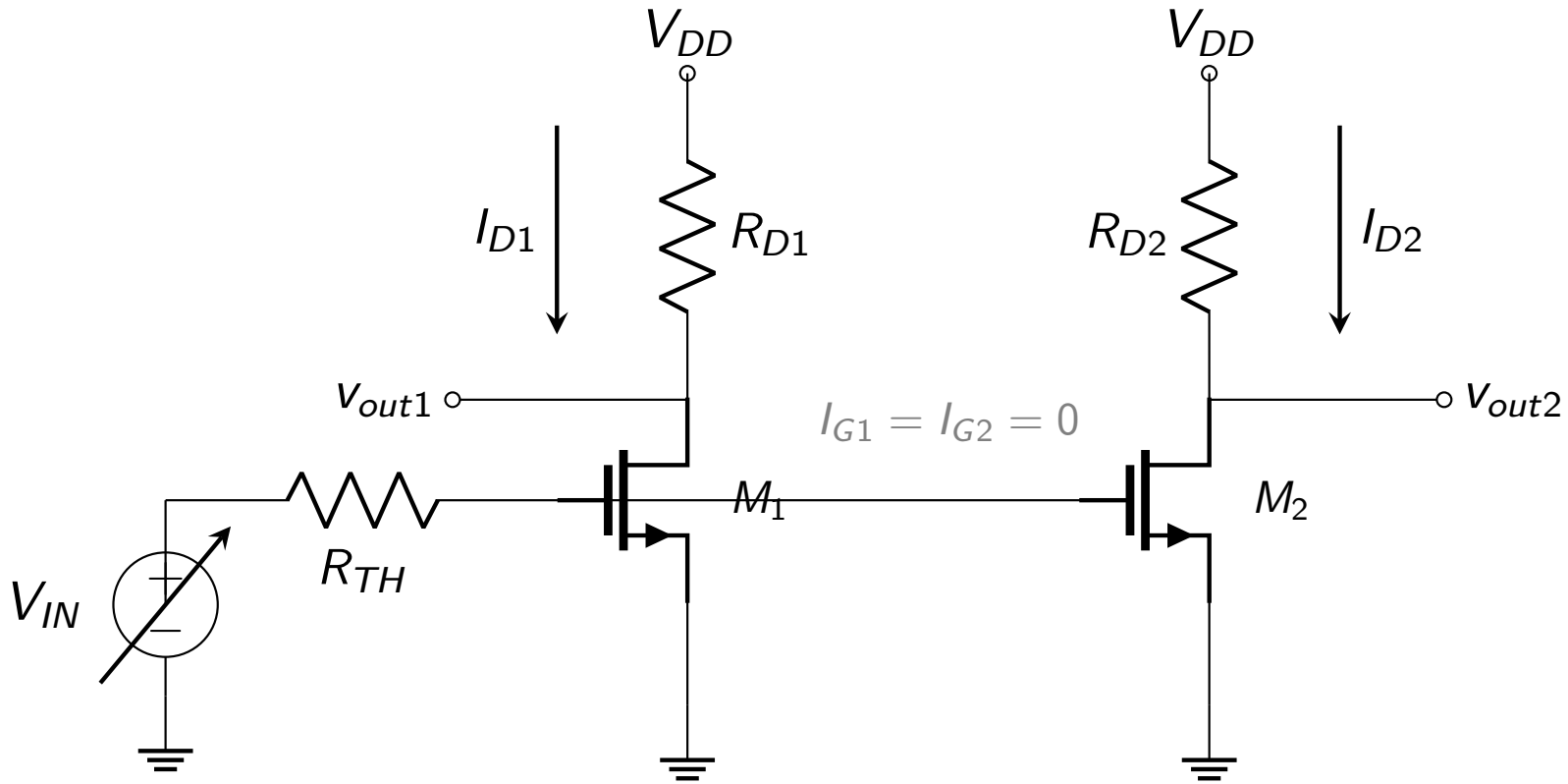
where $I_{DS} = (V_{DD} - V_{out})/R_D = 4/R_D$ at $V_{out} = 6$ V:

R_D (Ω)	I_{DS} (mA)	V_{IN} (V)	dV_{out}/dV_{IN}
200	20.0	2.700	-4.0
500	8.0	1.965	-6.3
1000	**4.0**	**1.594**	$\mathbf{-8.9}$
2000	2.0	1.332	-12.6
5000	0.8	1.100	-20.0

Compare with BJT: gain of -60.6 at same V_{out} with $R_C = 100\ \Omega$. MOSFET gain is much lower because $g_m = 2I_{DS}/(V_{GS} - V_{TN}) \ll I_C/V_T$ (BJT).

Parallel CS Amplifiers

Two CS Amplifiers Sharing One Source



Same parameters: $V_{DD} = 10$ V, $R_{D1} = R_{D2} = 1$ kΩ, $R_{TH} = 100$ Ω, $K_n = 10$ mA/V^2

Still using $V_{IN} = 1.700$ V (our single-MOSFET design)

KVL: Why R_{TH} Has No Effect

KVL around the input loop:

$$V_{IN} = V_{GS} + (I_{G1} + I_{G2}) \cdot R_{TH}$$

Since $I_{G1} = I_{G2} = 0$ (MOSFET gate draws no current):

$$\boxed{V_{IN} = V_{GS}}$$ regardless of how many MOSFETs are connected!

Compare with the BJT case:

$$V_{IN} = V_{BE} + 2\, I_{B1} \cdot R_{TH} \quad \text{(BJT — } R_{TH} \text{ matters!)}$$

Adding more MOSFETs does **not** change V_{GS} or I_{DS}.
The Q-point is **completely unchanged** from the single-MOSFET case!

Operating Point: No Change!

With $V_{IN} = 1.700$ V and $I_G = 0$:

	Single MOSFET	**Parallel MOSFETs (each)**
V_{GS}	1.700 V	1.700 V
I_{DS}	5.00 mA	5.00 mA
V_{DS}	5.00 V	5.00 V
R_{TH} drop	0 mV	0 mV

Every value is identical! Adding a parallel MOSFET has zero effect on V_{GS}, I_{DS}, or V_{DS}.

Compare with BJT: adding a second transistor caused I_B to drop by 38%!

SPICE Simulation — Single CS Amplifier

```
* Single CS Amplifier - Operating Point
Vdd vdd 0 DC 10
Vin in 0 DC 1.7
Rth in gate 100
M1 drain gate 0 0 NMOS_IDEAL W=100u L=1u
Rd vdd drain 1000
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

SPICE operating-point results:

V_{GS}	1.700 V
I_{DS}	5.00 mA
V_{DS}	5.00 V

Note: $V_{GS} = V_{IN} = 1.700$ V exactly — R_{TH} drops zero volts.

SPICE Simulation — Parallel CS Amplifiers

```
* Parallel CS Amplifiers - Operating Point
Vdd1 vdd1 0 DC 10
Vdd2 vdd2 0 DC 10
Vin in 0 DC 1.7
Rth in gate 100
M1 drain1 gate 0 0 NMOS_IDEAL W=100u L=1u
M2 drain2 gate 0 0 NMOS_IDEAL W=100u L=1u
Rd1 vdd1 drain1 1000
Rd2 vdd2 drain2 1000
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

SPICE operating-point results (each transistor):

V_{GS}	1.700 V
$I_{D1} = I_{D2}$	5.00 mA
$V_{DS1} = V_{DS2}$	5.00 V

Identical to the single-MOSFET case — confirmed by SPICE.

Numerical vs. SPICE Results

	Single MOSFET		**Parallel (each)**	
	Numerical	SPICE	Numerical	SPICE
V_{GS}	1.700 V	1.700 V	1.700 V	1.700 V
I_{DS}	5.00 mA	5.00 mA	5.00 mA	5.00 mA
V_{DS}	5.00 V	5.00 V	5.00 V	5.00 V

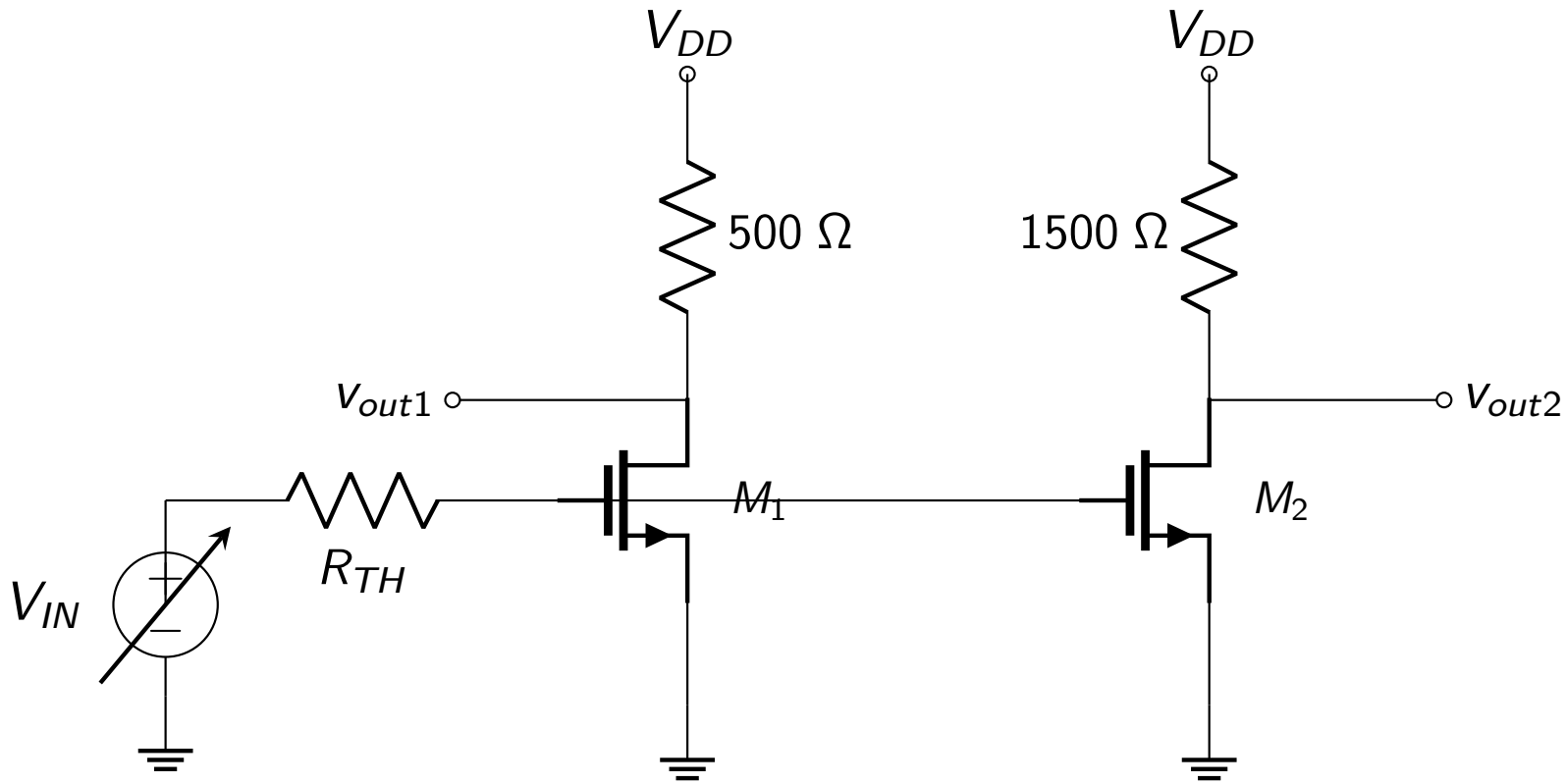
Numerical and SPICE results agree exactly.

No temperature correction needed (unlike BJT where we set $V_T = 26$ mV).

MOSFET $I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$ has no temperature-sensitive exponential.

What If $R_{D1} \neq R_{D2}$?

Parallel CS Amplifiers with Different R_D



Same transistors, same $V_{IN} = 1.700$ V, same $R_{TH} = 100\ \Omega$ — but $R_{D1} = 500\ \Omega$, $R_{D2} = 1500\ \Omega$

SPICE Simulation — Different R_D Values

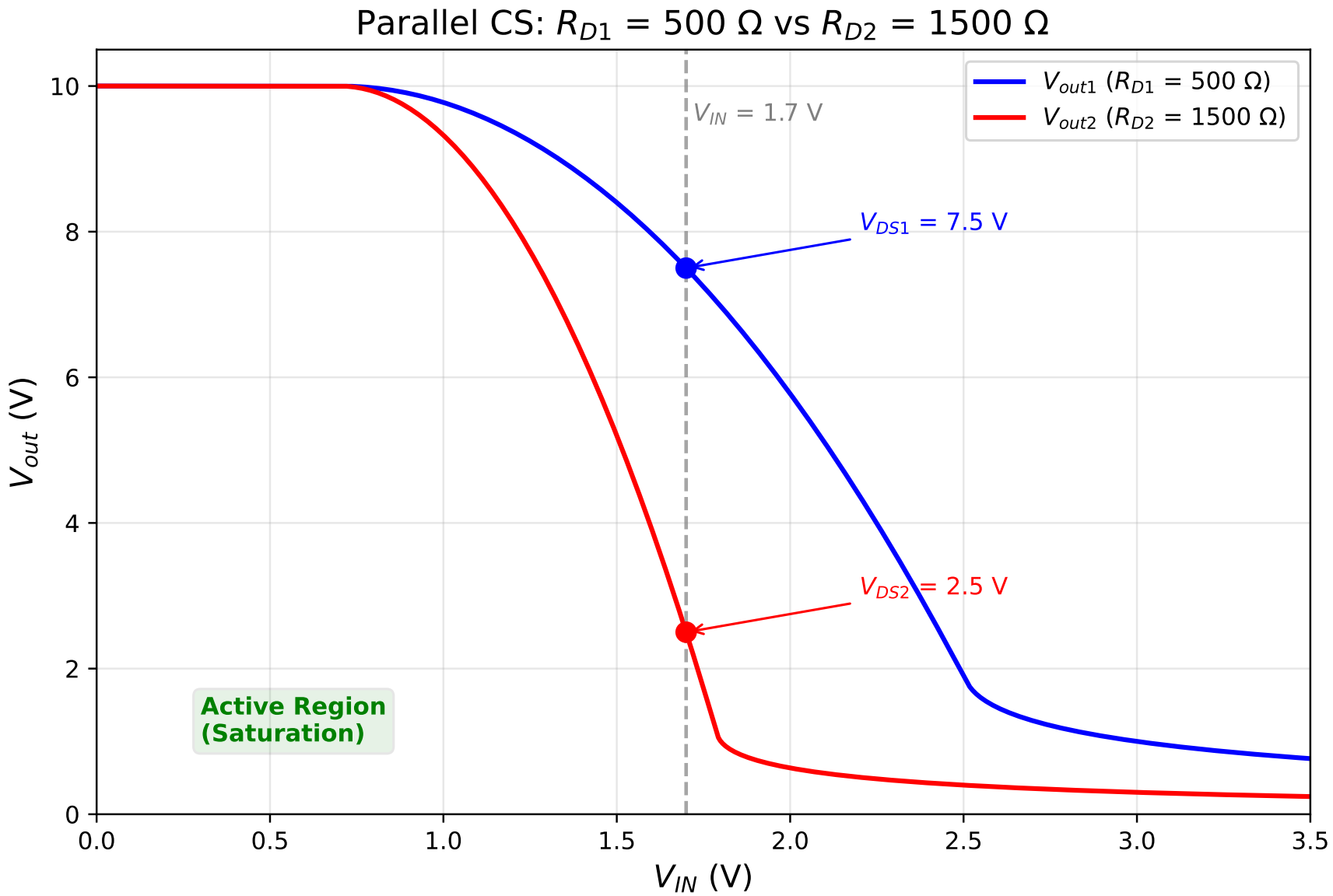
```
* Parallel CS - Different RD values
Vdd1 vdd1 0 DC 10
Vdd2 vdd2 0 DC 10
Vin in 0 DC 1.7
Rth in gate 100
M1 drain1 gate 0 0 NMOS_IDEAL W=100u L=1u
M2 drain2 gate 0 0 NMOS_IDEAL W=100u L=1u
Rd1 vdd1 drain1 500
Rd2 vdd2 drain2 1500
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

SPICE operating-point results:

	M_1 ($R_{D1} = 500\ \Omega$)	M_2 ($R_{D2} = 1500\ \Omega$)
V_{GS}	1.700 V	1.700 V
I_{DS}	5.00 mA	5.00 mA
V_{DS}	**7.50 V**	**2.50 V**

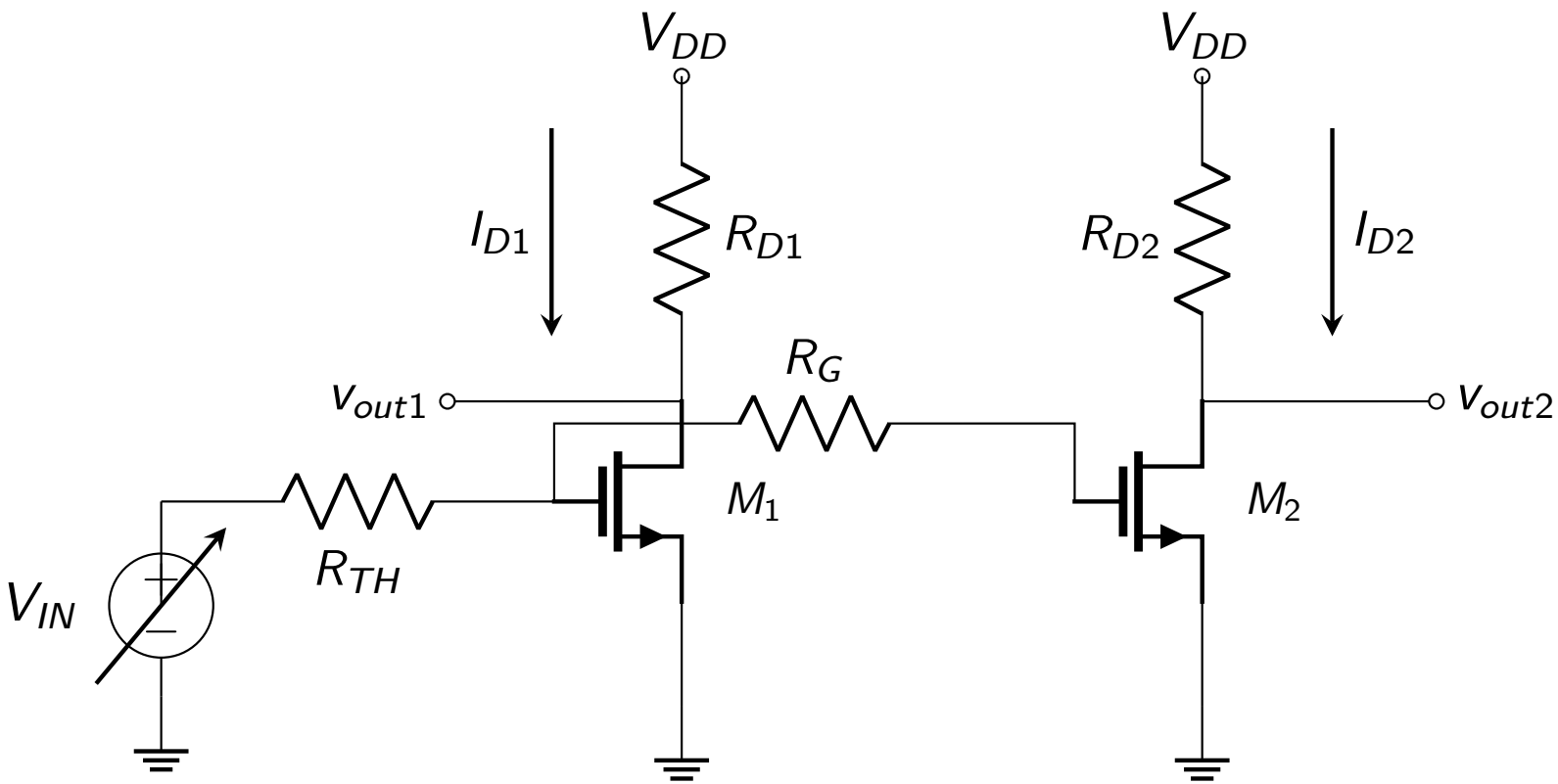
I_{DS} is **identical** — it depends only on V_{GS}, not on R_D. R_D only affects $V_{DS} = V_{DD} - I_{DS} \cdot R_D$.

Transfer Curves: $R_{D1} = 500\ \Omega$ vs. $R_{D2} = 1500\ \Omega$



Adding a Gate Resistor

Parallel CS with Resistor Between Gates



$R_{D1} = R_{D2} = 1\ \text{k}\Omega, \quad R_{TH} = 100\ \Omega, \quad R_G = 10\ \Omega, \quad V_{IN} = 1.700\ \text{V}$

SPICE Simulation — Gate Resistor $R_G = 10\ \Omega$

```
* Parallel CS with Gate Resistor
Vdd1 vdd1 0 DC 10
Vdd2 vdd2 0 DC 10
Vin in 0 DC 1.7
Rth in gate1 100
Rg gate1 gate2 10
M1 drain1 gate1 0 0 NMOS_IDEAL W=100u L=1u
M2 drain2 gate2 0 0 NMOS_IDEAL W=100u L=1u
Rd1 vdd1 drain1 1000
Rd2 vdd2 drain2 1000
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

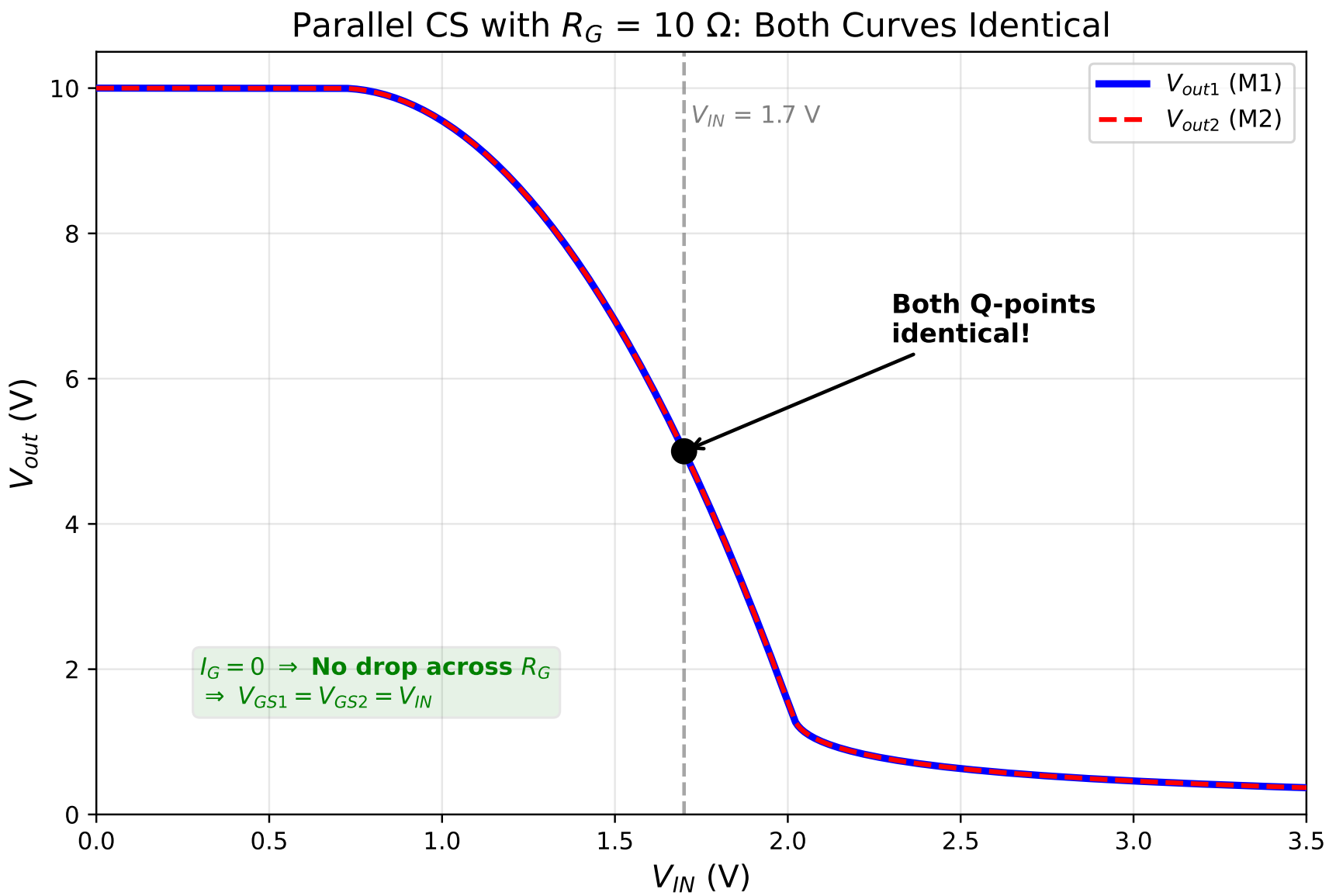
SPICE operating-point results:

	M_1	M_2
V_{GS}	1.700 V	1.700 V
I_{DS}	5.00 mA	5.00 mA
V_{DS}	5.00 V	5.00 V

R_G has **absolutely zero effect**! Since $I_G = 0$, there is no voltage drop across R_G.

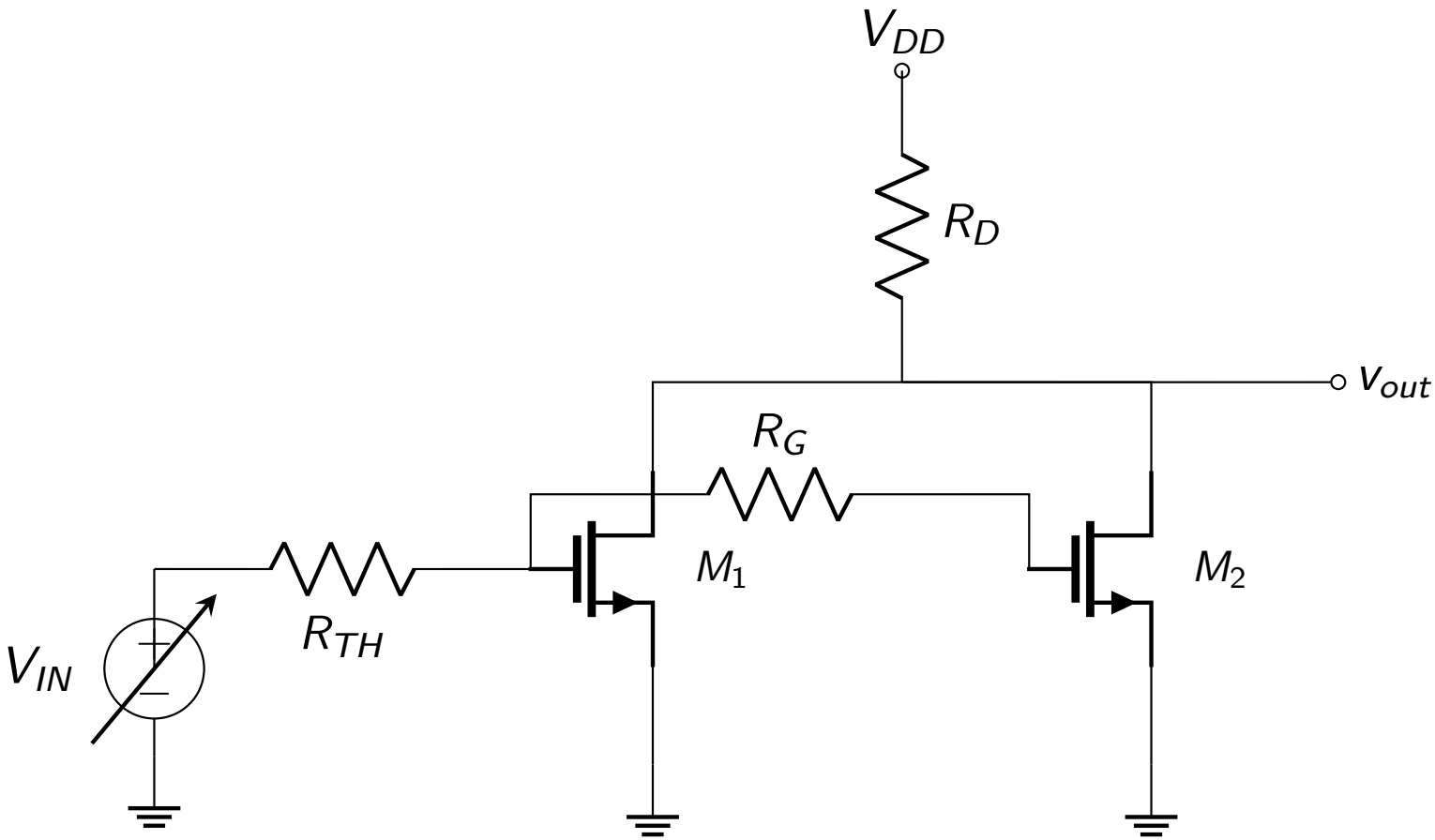
Compare with BJT: $R_B = 10\ \Omega$ caused a **12% current mismatch**!

Transfer Curves with $R_G = 10\ \Omega$ Between Gates



Merging to a Single R_D

Parallel CS with Shared R_D



$R_D = 1\ \text{k}\Omega, \quad R_{TH} = 100\ \Omega, \quad R_G = 10\ \Omega, \quad V_{IN} = 1.700\ \text{V}$

Now $I_{D,total} = I_{D1} + I_{D2}$ flows through a single R_D.

SPICE Simulation — Shared R_D

```
* Parallel CS - Gate Resistor, Single RD
Vdd vdd 0 DC 10
Vin in 0 DC 1.7
Rth in gate1 100
Rg gate1 gate2 10
M1 drain gate1 0 0 NMOS_IDEAL W=100u L=1u
M2 drain gate2 0 0 NMOS_IDEAL W=100u L=1u
Rd vdd drain 1000
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

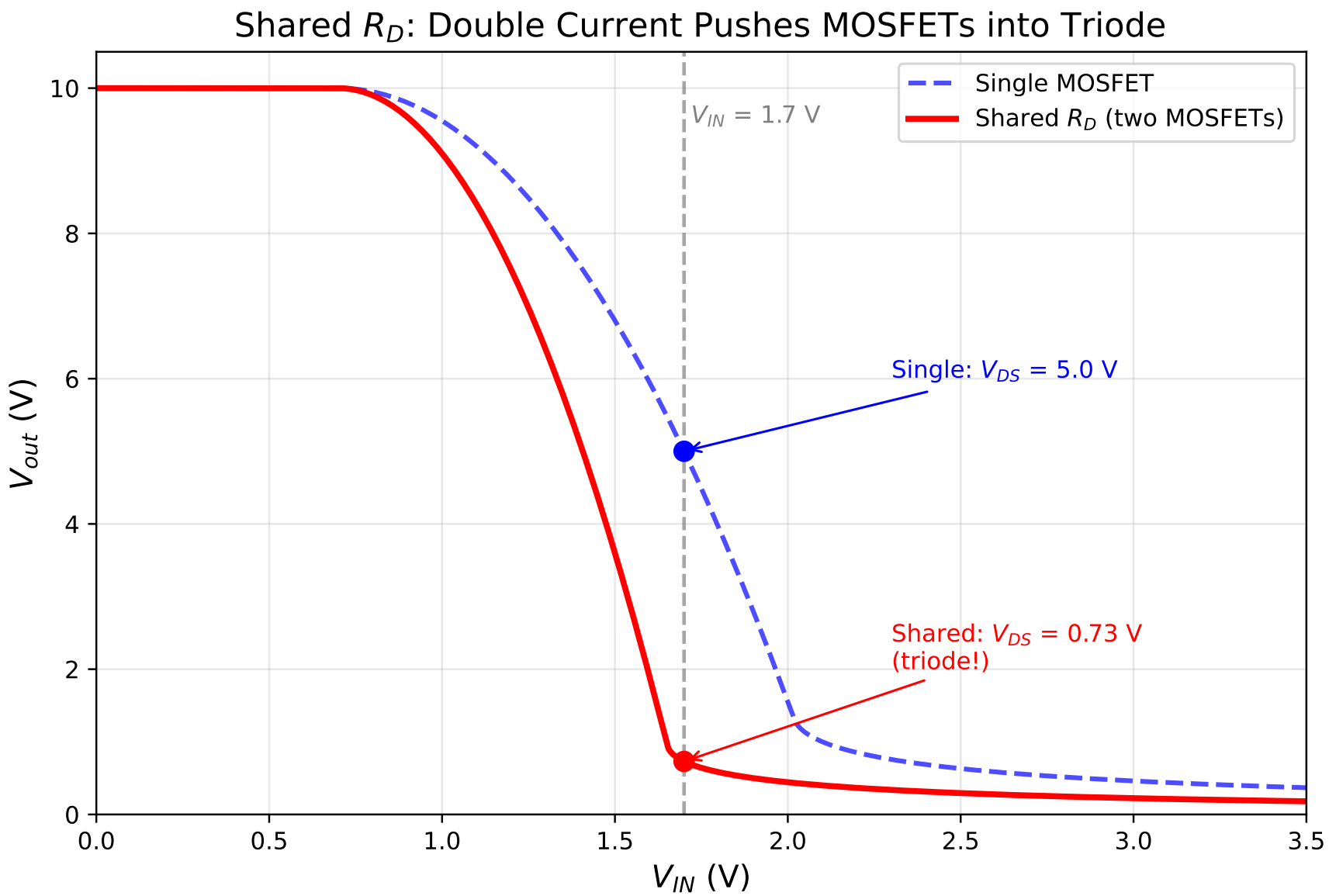
SPICE operating-point results:

	M_1	M_2
V_{GS}	1.700 V	1.700 V
I_{D1}, I_{D2}	4.64 mA	4.64 mA
$I_{D,total} = 9.27$ mA	$V_{DS} = V_{out} = 0.73$ V	

$V_{DS} = 0.73\ \text{V} < V_{GS} - V_{TN} = 1.0\ \text{V}$ — both MOSFETs are in **triode**!

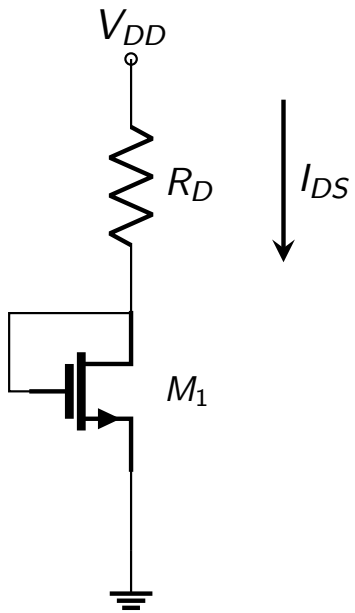
Since $I_G = 0$, there is no self-regulating mechanism like BJTs. The doubled current pushes V_{DS} below the saturation boundary.

Transfer Curve: Shared R_D



Gate-Drain Connected MOSFET

Gate-Drain Connected MOSFET

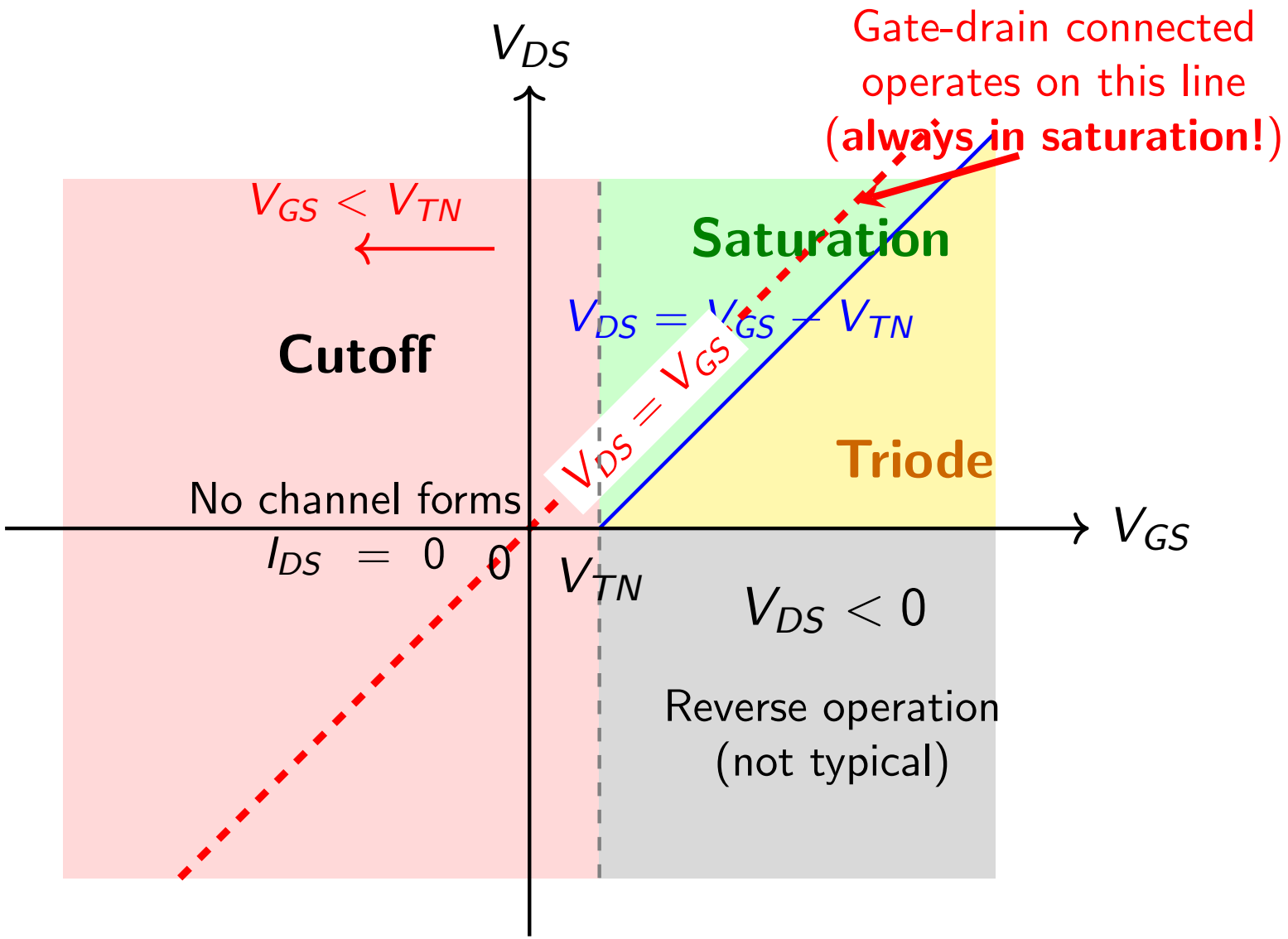


Gate tied to drain $\Rightarrow$ $V_G = V_D$ $\Rightarrow$ $V_{GS} = V_{DS}$

Since $V_{DS} = V_{GS} - V_{TN} + V_{TN} > V_{GS} - V_{TN}$, the MOSFET is **always in saturation**.

Circuit parameters: $V_{DD} = 10$ V, $R_D = 1$ kΩ, $K_n = 10$ mA/V^2, $V_{TN} = 0.7$ V

Why Gate-Drain Connected Is Always in Saturation



Setting Up the Equations

Since $V_G = V_D$ and $V_S = 0$:

$$V_{GS} = V_{DS} = V_D$$

KCL at the drain node (note: $I_G = 0$, so all current is I_{DS}):

$$\frac{V_{DD} - V_D}{R_D} = I_{DS} = \frac{K_n}{2}(V_{DS} - V_{TN})^2$$

Let $x = V_{DS} - V_{TN}$:

$$\boxed{\frac{K_n R_D}{2} x^2 + x - (V_{DD} - V_{TN}) = 0}$$

One equation, one unknown — solve by **quadratic formula** (no iteration needed!).

Solving by Quadratic Formula

With $\frac{K_n R_D}{2} = \frac{10 \times 10^{-3} \times 1000}{2} = 5$ and $V_{DD} - V_{TN} = 9.3$:

$$5x^2 + x - 9.3 = 0 \quad \Rightarrow \quad x = \frac{-1 + \sqrt{1 + 4(5)(9.3)}}{2(5)} = \frac{-1 + \sqrt{187}}{10}$$

$$x = \frac{-1 + 13.675}{10} = 1.268 \text{ V}$$

Solution:

$V_G = V_D = V_{GS} = V_{DS}$	1.968 V
V_S	0 V
I_{DS}	8.03 mA

No iteration needed! Unlike the BJT's transcendental equation $I_C = I_S e^{V_{BE}/V_T}$, the MOSFET's square-law gives a simple quadratic.

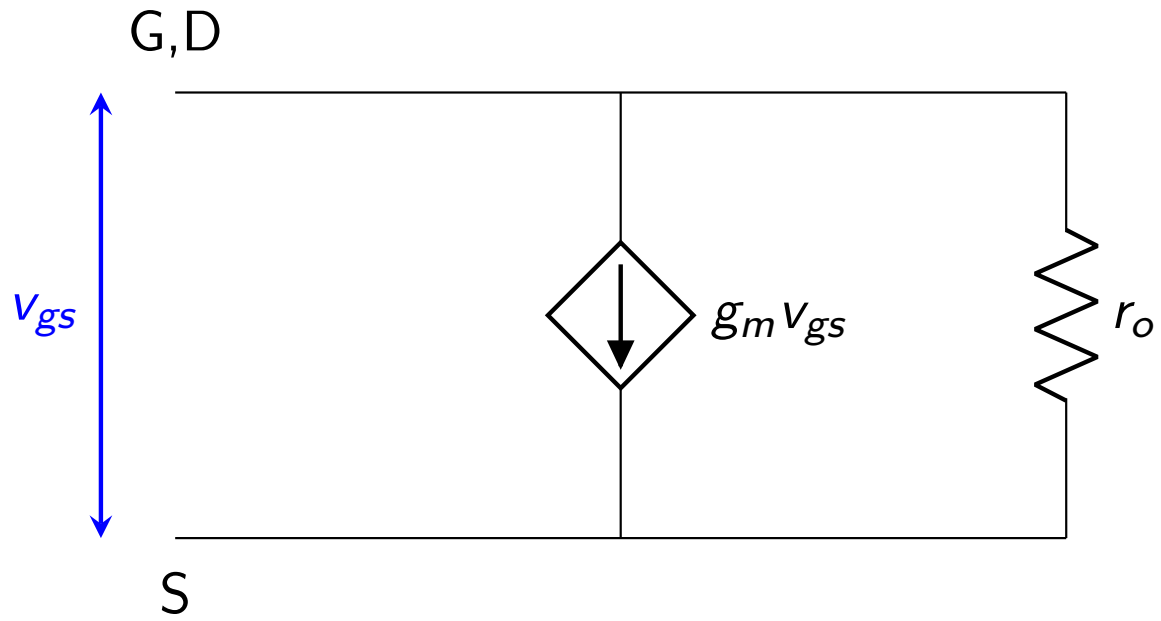
SPICE Verification

```
* Gate-Drain Connected MOSFET
Vdd vdd 0 DC 10
Rd vdd drain 1000
M1 drain drain 0 0 NMOS_IDEAL W=100u L=1u
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

	Numerical	SPICE
$V_G = V_D = V_{GS} = V_{DS}$	1.968 V	1.967 V
V_S	0 V	0 V
I_{DS}	8.03 mA	8.03 mA

Numerical and SPICE agree (minor rounding in V_{DS}).

Small-Signal Model: Gate-Drain Connected MOSFET



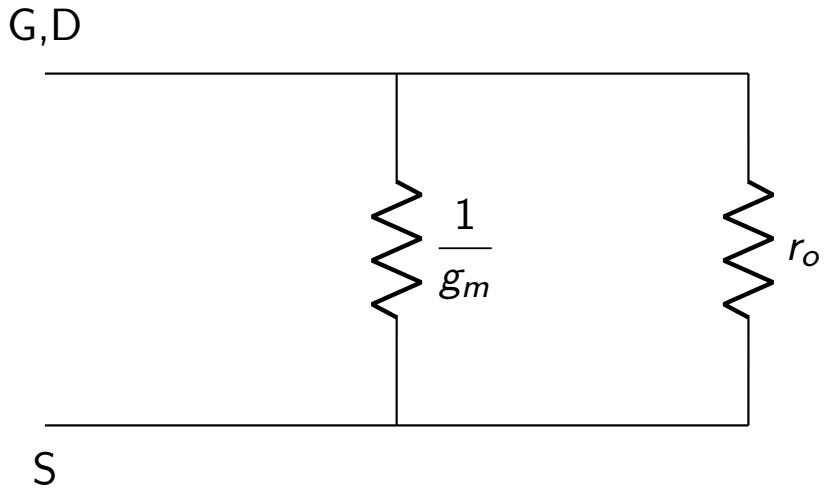
Since G and D are tied together, $v_{gs} = v_{ds}$ appears across both elements:

- $g_m v_{gs}$: current $= g_m \cdot v_{gs}$ (directly proportional to v_{gs}!)
- r_o: current $= v_{gs} \,/\, r_o$ (Ohm's law)

The dependent source $g_m v_{gs}$ acts like a **resistor** $1/g_m$, because v_{gs} is the voltage across it.

No r_π — the MOSFET gate draws no current!

Replacing $g_m v_{gs}$ with $1/g_m$



Two resistors in parallel — combine into one equivalent:

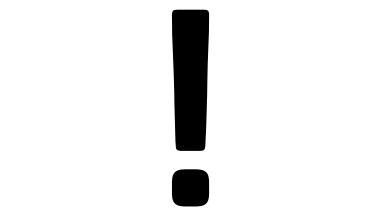
$$\boxed{r_{eq} = \frac{1}{g_m} \parallel r_o}$$

With $I_{DS} = 8.03$ mA and $\lambda = 0.02$:
$g_m = K_n(V_{GS} - V_{TN}) = (10 \times 10^{-3})(1.268) = 12.68$ mS
$r_o = 1/(\lambda I_{DS}) = 1/(0.02 \times 8.03 \times 10^{-3}) = 6227\ \Omega$

$$r_{eq} = 78.9 \parallel 6227 = 77.9\ \Omega \approx \frac{1}{g_m} = 78.9\ \Omega$$

Simpler than BJT: no r_π term! Just $1/g_m \parallel r_o$.

$r_{eq} \approx 1/g_m = V_{ov}/(2I_{DS})$ where $V_{ov} = V_{GS} - V_{TN}$.
The gate-drain connected MOSFET looks like a **small resistance** to ground.



Tying the gate to the drain creates an

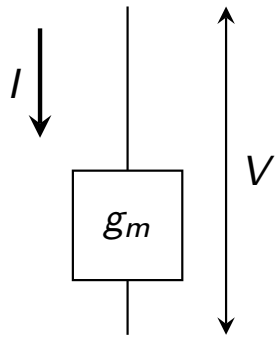
ACTIVE LOAD

Large signal: acts like a **non-linear** resistor

Small signal: acts **exactly** like a resistor $r_{eq} \approx 1/g_m$

Full Circle: The Square-Law Device from Lecture 1

Lecture 1: Square-Law Device

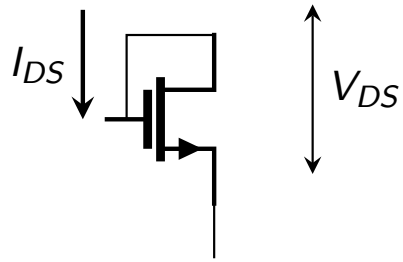


$$I = g_m(V - V_t)^2$$

$$r = \frac{1}{2\,g_m(V - V_t)}$$

$=$

Lecture 10: Gate-Drain MOSFET



$$I_{DS} = \frac{K_n}{2}(V_{DS} - V_{TN})^2$$

$$r_{eq} \approx \frac{1}{K_n(V_{DS} - V_{TN})}$$

They are the same device! $g_m \leftrightarrow K_n/2$, $V_t \leftrightarrow V_{TN}$, $V \leftrightarrow V_{DS} = V_{GS}$

The gate-drain connected MOSFET **is** the two-terminal square-law device.