

EE461g: Introduction to Electronic Circuits

Lecture 11

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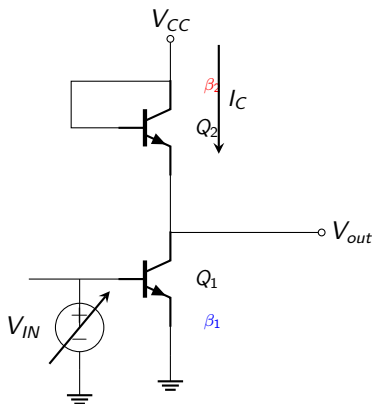
University of Kentucky

Outline

- 1 CE Amplifier with Active Load
- 2 CS Amplifier with Active Load
- 3 Small-Signal Analysis
- 4 Summary
- 5 CC Amplifier (Emitter Follower)
- 6 MOSFET Source Follower (Common Drain)

CE Amplifier with Active Load

CE Amplifier with Diode-Connected Load



Q_2 is **diode-connected** (base tied to collector). Q_1 amplifies; Q_2 serves as the active load.

$$V_{CC} = 10 \text{ V}, \quad I_S = 10^{-14} \text{ A}, \quad \beta_1 = \beta_2 = 100, \quad V_T = 26 \text{ mV}$$

Large-Signal Analysis

KCL at V_{out} : $I_{E2} = I_{C1}$

Q_2 diode-connected: $I_{E2} = I_{C2} \frac{\beta_2 + 1}{\beta_2}$

Q_1 collector: $I_{C1} = I_S e^{V_{IN}/V_T}$

Q_2 collector: $I_{C2} = I_S e^{(V_{CC}-V_{out})/V_T}$

Substituting $I_{E2} = I_{C1}$:

$$I_S e^{(V_{CC}-V_{out})/V_T} \cdot \frac{\beta_2 + 1}{\beta_2} = I_S e^{V_{IN}/V_T}$$

$$V_{out} = V_{CC} - V_{IN} + V_T \ln\left(\frac{\beta_2 + 1}{\beta_2}\right)$$

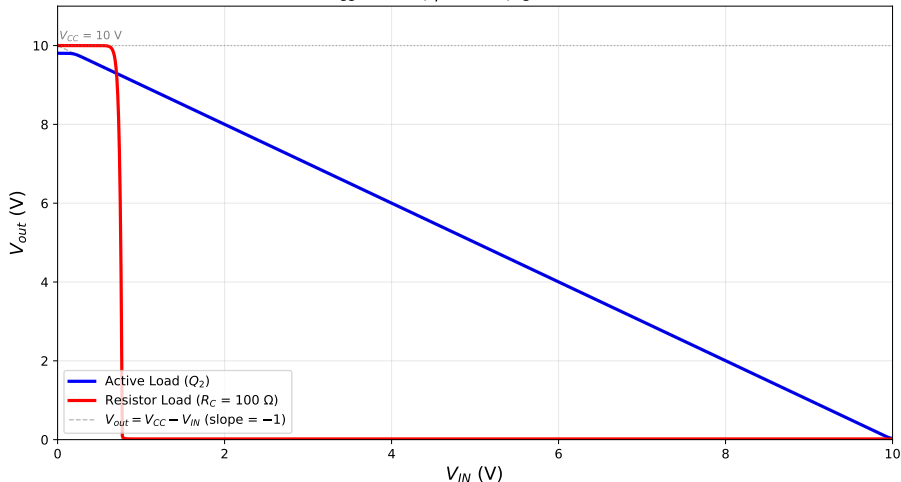
$V_T \ln(101/100) = 0.26 \text{ mV}$ — negligible! $\Rightarrow$ **slope** = -1 , independent of β_1 and β_2 .

Note: β_1 does not appear at all!

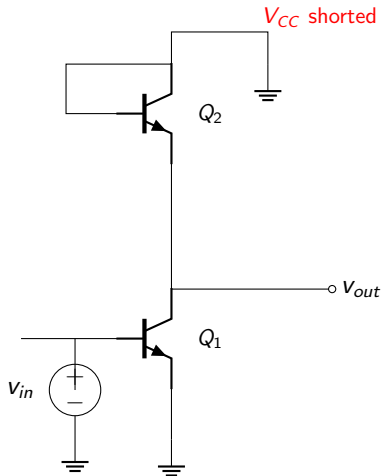
Transfer Curve: Active Load vs Resistor Load

CE Amplifier: Active Load vs Resistor Load (SPICE)

$V_{CC} = 10\text{ V}$, $\beta = 100$, $I_S = 10^{-14}\text{ A}$

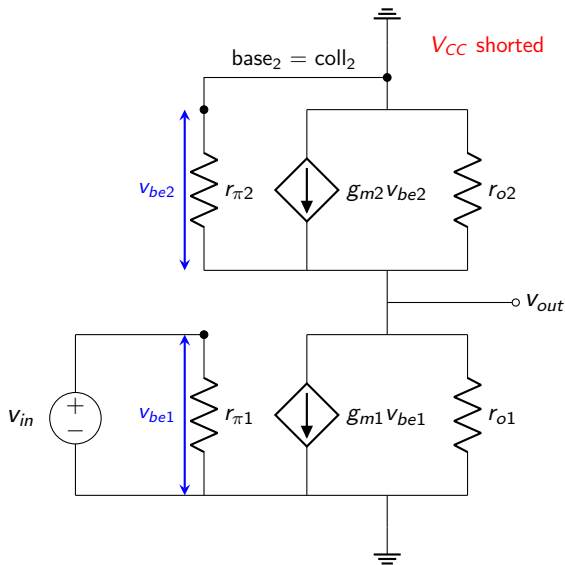


Small-Signal Step 1: Short DC Sources

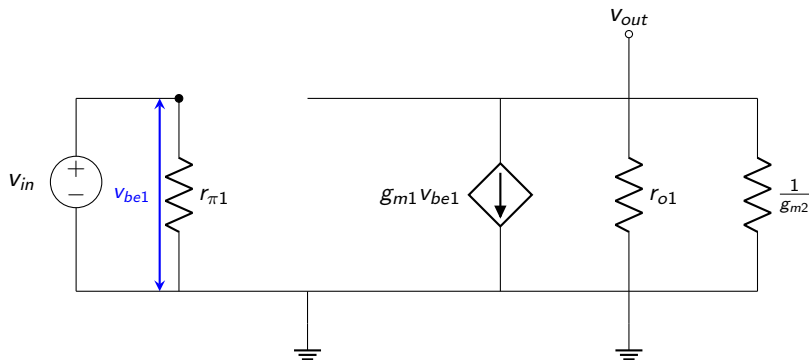


Short V_{CC} to ground. Q_2 's collector/base is at AC ground. Looking into Q_2 's emitter: resistance $= r_{e2} = \frac{\beta_2}{(\beta_2 + 1) g_{m2}}$.

Small-Signal Step 2: Hybrid- π Models



Small-Signal Step 3: Simplified Equivalent Circuit



- Q_1 : full hybrid- π model (has $r_{\pi 1}$ because BJT base draws current)
- Q_2 diode-connected $\Rightarrow$ resistance looking into emitter $\approx 1/g_{m2}$ (Lecture 8)

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\frac{g_{m1}}{g_{m2}} = -\frac{I_{C1}/V_T}{I_{C2}/V_T} = -\frac{I_{C1}}{I_{C2}}$$

What Controls I_{C1}/I_{C2} ?

$$I_{C1} = I_{S1} e^{V_{BE1}/V_T}, \quad I_{C2} = I_{S2} e^{V_{BE2}/V_T}$$

Can we manipulate I_{S1} , I_{S2} (transistor area) to set the gain?

No. KCL forces:

$$I_{C1} = I_{E2} = I_{C2} \frac{\beta_2 + 1}{\beta_2} \Rightarrow \frac{I_{C1}}{I_{C2}} = \frac{\beta_2 + 1}{\beta_2} \approx 1 \text{ always}$$

Changing I_{S1}/I_{S2} only shifts the V_{BE} 's to maintain this ratio.

$$A_v = -\frac{I_{C1}}{I_{C2}} = -\frac{\beta_2 + 1}{\beta_2} \approx -1$$

No design knob — gain is always -1 .

CE Active Load: Summary

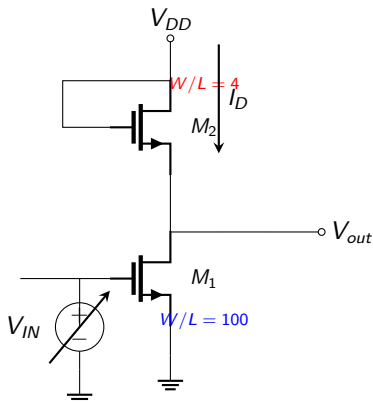
	Active Load (diode-connected Q_2)	Resistor Load ($R_C = 100\ \Omega$)
Large-signal	$V_{out} \approx V_{CC} - V_{IN}$	nonlinear
Slope	-1	varies with I_C
Small-signal A_v	-1	$-g_m R_C$
β dependence	none	A_v independent of β

Key insight: The diode-connected BJT active load gives $|A_v| = 1$ exactly, regardless of β_1 or β_2 .

This is the BJT analog of the MOSFET result with identical M_1, M_2 .

CS Amplifier with Active Load

CS Amplifier with Diode-Connected Load



R_D is **replaced** by diode-connected M_2 (gate tied to drain). M_2 has a **smaller** W/L than M_1 .

$$V_{DD} = 10 \text{ V}, \quad K_{n1} = 10 \text{ mA/V}^2, \quad K_{n2} = 0.4 \text{ mA/V}^2, \quad V_{TN} = 0.7 \text{ V}, \quad \lambda = 0$$

Large-Signal Analysis

KCL at the V_{out} node: $I_{D1} = I_{D2}$

M_1 in saturation:

$$I_{D1} = \frac{K_{n1}}{2}(V_{IN} - V_{TN})^2$$

M_2 diode-connected ($V_{GS2} = V_{DD} - V_{out}$):

$$I_{D2} = \frac{K_{n2}}{2}(V_{DD} - V_{out} - V_{TN})^2$$

Setting $I_{D1} = I_{D2}$ with $K_{n1} \neq K_{n2}$:

$$V_{DD} - V_{out} - V_{TN} = \sqrt{\frac{K_{n1}}{K_{n2}}}(V_{IN} - V_{TN})$$

$$V_{out} = V_{DD} - V_{TN} - \sqrt{\frac{K_{n1}}{K_{n2}}}(V_{IN} - V_{TN})$$

Large-Signal: Numerical Example

With $K_{n1}/K_{n2} = 10 \text{ mA/V}^2 / 0.4 \text{ mA/V}^2 = 25$:

$$\sqrt{K_{n1}/K_{n2}} = 5$$

$$V_{out} = 10 - 0.7 - 5(V_{IN} - 0.7) = 13.5 - 5 V_{IN}$$

At $V_{IN} = 1.7 \text{ V}$:

$$V_{out} = 13.5 - 5(1.7) = 4.3 \text{ V}$$

$$\text{Slope} = -\sqrt{K_{n1}/K_{n2}} = -5$$

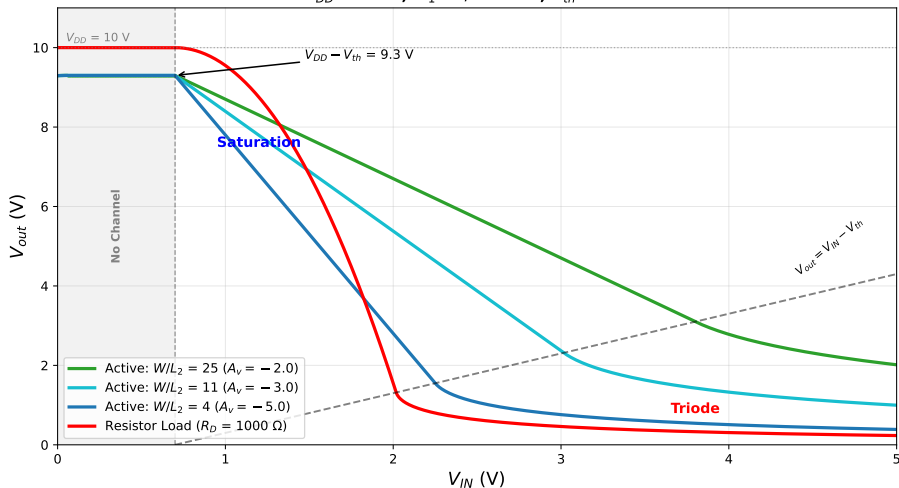
Compare: with identical M_2 ($W/L = 100$), slope = -1 .

With $R_D = 1 \text{ k}\Omega$, slope at $V_{IN} = 1.7 \text{ V}$ is $-K_{n1}(V_{IN} - V_{TN})R_D = -10$.

Transfer Curve: Active Load vs Resistor Load

CS Amplifier: Active Load vs Resistor Load (SPICE)

$V_{DD} = 10\text{ V}$, M_1 : $W/L = 100$, $V_{th} = 0.7\text{ V}$



Operating Regions of M_1

Peak $V_{out} = V_{DD} - V_{TN} = 9.3 \text{ V}$ (not 10 V) because M_2 needs at least V_{TN} across its gate-source before any current can flow.

- **No Channel** ($V_{IN} < V_{TN}$): M_1 is off, $I_D = 0$.
- **Saturation** ($V_{IN} > V_{TN}$, $V_{out} \geq V_{IN} - V_{TN}$):
 M_1 acts as a current source. Linear transfer curve, constant slope.
- **Triode** ($V_{out} < V_{IN} - V_{TN}$):
 M_1 acts as a resistor. Curve bends and V_{out} flattens toward 0.

The **saturation** region is where the amplifier operates. Higher gain (smaller W/L_2) $\Rightarrow$ narrower saturation region $\Rightarrow$ less output swing.

SPICE Verification — CS with Active Load

```
* CS Amplifier with Active Load
Vdd vdd 0 DC 10
Vin gate1 0 DC 1.7
M1 vout gate1 0 0 NMOS_IDEAL W=100u L=1u
M2 vdd vdd vout 0 NMOS_IDEAL W=4u L=1u
.model NMOS_IDEAL NMOS(VTO=0.7 KP=100u LAMBDA=0)
```

Operating-point results (at $V_{IN} = 1.7$ V):

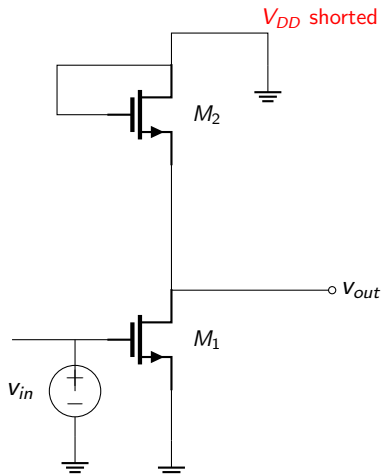
	M_1 ($W/L = 100$)	M_2 ($W/L = 4$)
V_{GS}	1.700 V	5.700 V
I_D	5.00 mA	5.00 mA
V_{DS}	4.30 V	5.700 V

$$V_{out} = V_{DD} - V_{GS2} = 10 - 5.7 = 4.3 \text{ V} \quad \checkmark$$

Small-Signal Analysis

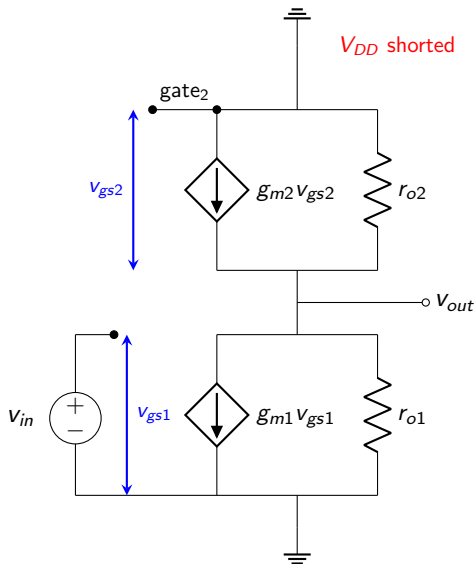
CS with Active Load

Step 1: Short DC Sources

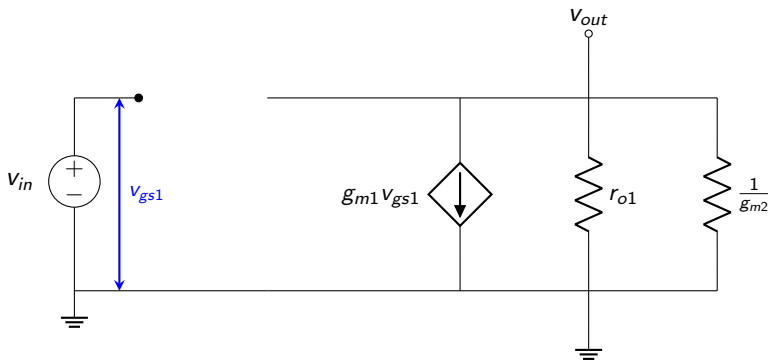


Short V_{DD} to ground. M_2 's drain is at AC ground. Looking into M_2 's source: equivalent resistance $\approx 1/g_{m2}$.

Step 2: Replace Each Transistor with Its Model



Step 3: Simplified Equivalent Circuit



- M_1 : MOSFET model — no r_{π} (gate draws zero current)
- M_2 diode-connected: looking into source $\Rightarrow$ resistance $\approx 1/g_{m2}$
- With $\lambda = 0$: $r_{o1} \rightarrow \infty$, so load = $1/g_{m2}$

Voltage Gain Derivation

The voltage gain is:

$$A_v = -g_{m1} \left(\frac{1}{g_{m2}} \parallel r_{o1} \right)$$

With $\lambda = 0$ ($r_{o1} \rightarrow \infty$):

$$A_v = -\frac{g_{m1}}{g_{m2}}$$

Since $I_{D1} = I_{D2} = I_D$, use $g_m = \sqrt{2K_n I_D}$:

$$A_v = -\frac{\sqrt{2K_{n1} I_D}}{\sqrt{2K_{n2} I_D}}$$

$$A_v = -\sqrt{\frac{K_{n1}}{K_{n2}}} = -\sqrt{25} = -5$$

Comparison: Active Load vs Resistor Load

	Active	Active	Resistor
	$(M_2 = M_1)$	$(M_2: W/L = 4)$	$(R_D = 1 \text{ k}\Omega)$
Load	$\frac{1}{g_{m2}} = 100 \text{ }\Omega$	$\frac{1}{g_{m2}} = 500 \text{ }\Omega$	$R_D = 1000 \text{ }\Omega$
Gain	-1	-5	-10

Key insight: Making M_2 smaller increases $1/g_{m2}$, which increases gain.

$$\frac{1}{g_{m2}} = \frac{1}{K_{n2}(V_{GS2} - V_{TN})} \quad \text{— smaller } K_{n2} \Rightarrow \text{larger } 1/g_{m2} \Rightarrow \text{larger } |A_v|$$

Summary

Active Load Gain Is Controlled by W/L Ratio

The CS amplifier with a diode-connected NMOS load has:

$$A_v = -\sqrt{\frac{K_{n1}}{K_{n2}}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

- **Identical transistors:** $A_v = -1$ (load “undoes” the gain)
- **Smaller M_2 :** $|A_v|$ increases (e.g., W/L ratio of 25 $\Rightarrow A_v = -5$)
- **Limitation:** Larger gain $\Rightarrow$ smaller V_{out} swing (headroom)

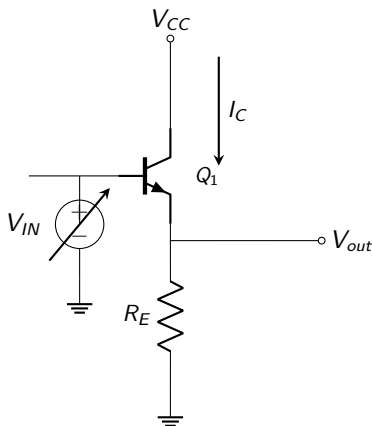
Coming up: Use a **PMOS current source** (not diode-connected)

as the load for much higher gain: $A_v = -g_m(r_{o,n} \parallel r_{o,p}) \gg 1$

CC Amplifier

(Emitter Follower)

Common Collector: Circuit



Input at the **base**, output at the **emitter**, collector tied to V_{CC} . The collector is the **common** terminal $\Rightarrow$ “Common Collector.”

$$V_{CC} = 10 \text{ V}, \quad R_E = 1 \text{ k}\Omega, \quad \beta = 100, \quad I_S = 10^{-14} \text{ A}$$

Large-Signal: Iterative Solution

Assume Q_1 is in the **active** region. KVL gives:

$$V_{IN} = V_{BE} + V_{out}, \quad V_{out} = I_E R_E, \quad I_C = I_S e^{V_{BE}/V_T}, \quad I_E = I_C \frac{\beta + 1}{\beta}$$

Procedure: guess V_{BE} , compute forward, update V_{BE} .

Example: $V_{IN} = 5$ V, guess $V_{BE}^{(0)} = 0.700$ V.

Iter	V_{BE} (V)	V_{out} (V)	I_E (mA)	I_C (mA)	V_{BE}^{new} (V)
0	0.700	4.300	4.300	4.257	0.696
1	0.696	4.304	4.304	4.261	0.696 ✓

$V_{BE}^{new} = V_T \ln(I_C/I_S)$. Converges in **one iteration** because V_{BE} changes only 4 mV!

Large-Signal: V_{out} vs V_{IN}

Converged iterative solution for each V_{IN} :

V_{IN} (V)	V_{BE} (V)	V_{out} (V)	$V_{IN} - 0.7$ (V)
1	0.632	0.368	0.300
2	0.666	1.334	1.300
3	0.680	2.320	2.300
4	0.689	3.311	3.300
5	0.696	4.304	4.300
6	0.702	5.298	5.300
7	0.706	6.294	6.300
8	0.710	7.290	7.300
9	0.713	8.287	8.300
10	0.716	9.284	9.300

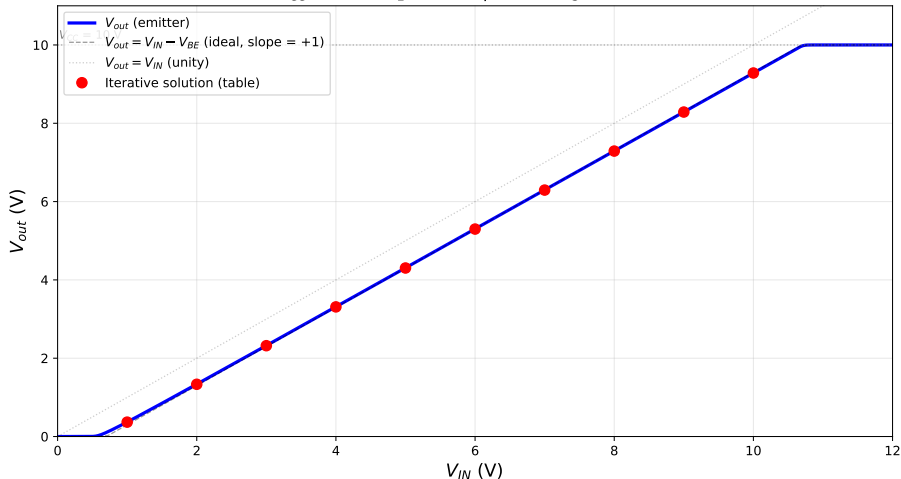
V_{BE} ranges from 0.632 to 0.716 V (only 84 mV over 9 V of V_{IN}).

$V_{out} \approx V_{IN} - 0.7$ V Slope $\approx +1$ (non-inverting) $\Rightarrow$ “emitter follower”

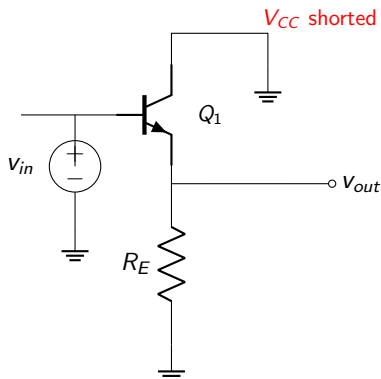
Transfer Curve (SPICE)

Common Collector (Emitter Follower): V_{out} vs V_{in} (SPICE)

$V_{CC} = 10\text{ V}$, $R_E = 1\text{ k}\Omega$, $\beta = 100$, $I_S = 10^{-14}\text{ A}$

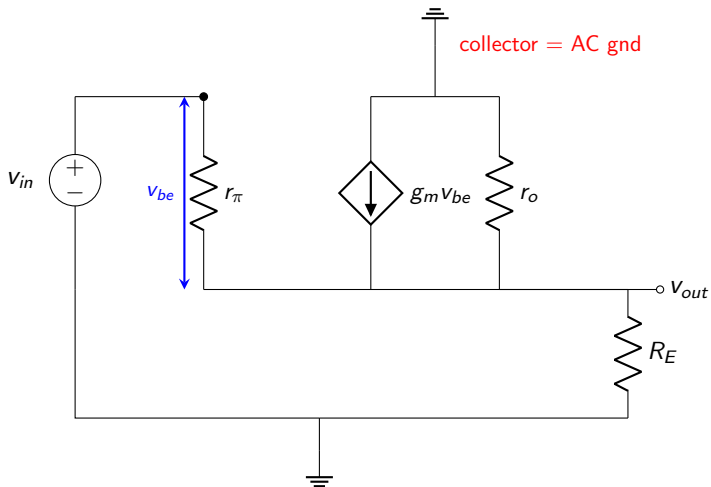


Small-Signal Step 1: Short DC Sources

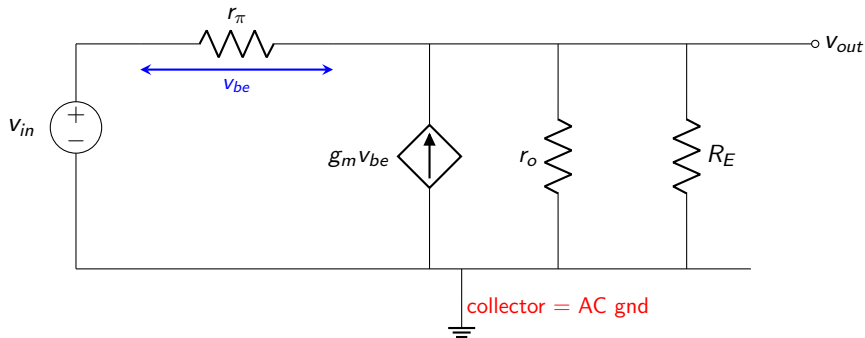


Short V_{CC} to ground. Collector is at AC ground. Output is at the emitter — this is a **common collector** configuration.

Small-Signal Step 2: Hybrid- π Model



Small-Signal Step 3: Rearranged Model



$g_m V_{be}$, r_o , and R_E are all in parallel between v_{out} and ground.

Voltage Gain Derivation

From the circuit: $v_{be} = v_{in} - v_{out}$

KCL at v_{out} (ignoring r_o): current from $g_m v_{be}$ plus current through r_π flows through R_E :

$$v_{out} = \left(g_m v_{be} + \frac{v_{be}}{r_\pi} \right) R_E$$

Replace $v_{be} = v_{in} - v_{out}$:

$$v_{out} = \left(g_m + \frac{1}{r_\pi} \right) (v_{in} - v_{out}) R_E$$

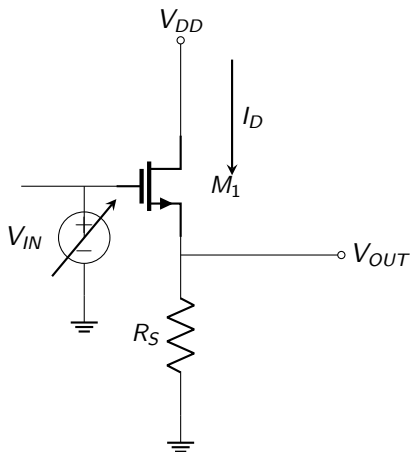
Solving for v_{out}/v_{in} :

$$A_v = \frac{\left(g_m + \frac{1}{r_\pi} \right) R_E}{1 + \left(g_m + \frac{1}{r_\pi} \right) R_E} \approx 1$$

$A_v < 1$ always, but $\rightarrow 1$ when $g_m R_E \gg 1$. **Non-inverting**, gain $\approx +1$.

MOSFET Source Follower (Common Drain)

Common Drain Circuit



Input at the **gate**, output at the **source**, drain tied to V_{DD} . The drain is the **common** terminal $\Rightarrow$ “Common Drain.”

$$V_{DD} = 10 \text{ V}, \quad R_S = 1 \text{ k}\Omega, \quad K_n = 10 \text{ mA/V}^2, \quad V_{TN} = 0.7 \text{ V}$$

Large-Signal Analysis

Assume M_1 is in **saturation** ($V_{DS} \geq V_{GS} - V_{TN}$):

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2, \quad V_{GS} = V_{IN} - V_{OUT}, \quad V_{OUT} = I_D \cdot R_S$$

Substituting:

$$\frac{V_{OUT}}{R_S} = \frac{K_n}{2}(V_{IN} - V_{OUT} - V_{TN})^2$$

This is a **quadratic** in V_{OUT} — no simple closed-form like the BJT.

Key difference from BJT: V_{GS} varies significantly with I_D (square-law), while V_{BE} is nearly constant (exponential).

⇒ The MOSFET source follower has slope < 1 , not ≈ 1 .

Large-Signal: Iterative Solution

Procedure: guess V_{GS} , compute forward, update.

$$V_{GS}^{\text{new}} = V_{TN} + \sqrt{2 I_D / K_n}, \quad \text{where } I_D = V_{OUT} / R_S.$$

Example: $V_{IN} = 5$ V, guess $V_{GS}^{(0)} = 1.000$ V.

Iter	V_{GS} (V)	V_{OUT} (V)	I_D (mA)	V_{GS}^{new} (V)
0	1.000	4.000	4.000	1.594
1	1.594	3.406	3.406	1.525
2	1.525	3.475	3.475	1.534
3	1.534	3.466	3.466	1.533
4	1.533	3.467	3.467	1.533 ✓

Compare BJT at $V_{IN} = 5$ V: $V_{BE} = 0.696$ V, $V_{OUT} = 4.304$ V.

MOSFET: $V_{GS} = 1.533$ V, $V_{OUT} = 3.467$ V. **Much larger voltage drop!**

Large-Signal: V_{OUT} vs V_{IN}

Converged iterative solution for each V_{IN} :

V_{IN} (V)	V_{GS} (V)	V_{OUT} (V)	$V_{IN} - V_{TN}$ (V)
1	0.865	0.135	0.300
2	1.120	0.880	1.300
3	1.286	1.714	2.300
4	1.419	2.581	3.300
5	1.533	3.467	4.300
6	1.634	4.366	5.300
7	1.727	5.273	6.300
8	1.812	6.188	7.300
9	1.892	7.108	8.300
10	1.967	8.033	9.300

V_{GS} ranges from 0.865 to 1.967 V (**over 1.1 V** of variation!)

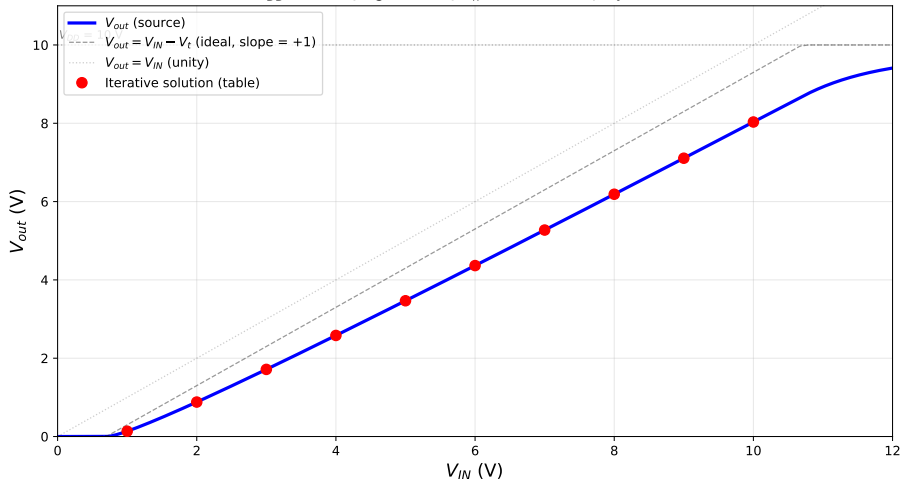
Compare BJT: V_{BE} ranged from 0.632 to 0.716 V (only 84 mV).

V_{OUT} is always **below** $V_{IN} - V_{TN}$ because $V_{GS} > V_{TN}$ (needs overdrive).

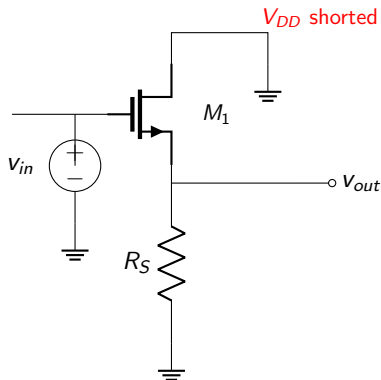
Transfer Curve (SPICE)

Common Drain (Source Follower): V_{out} vs V_{IN} (SPICE)

$V_{DD} = 10\text{ V}$, $R_S = 1\text{ k}\Omega$, $k_n = 10\text{ mA/V}^2$, $V_t = 0.7\text{ V}$



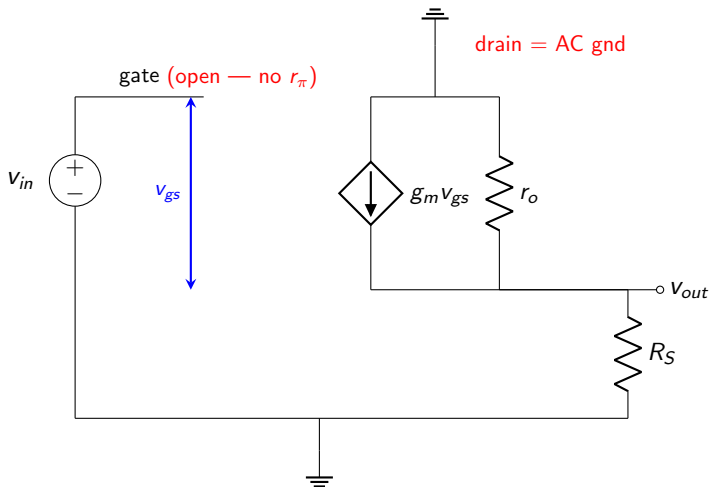
Small-Signal Step 1: Short DC Sources



Short V_{DD} to ground. Drain is at AC ground. Output is at the source — this is a **common drain** configuration.

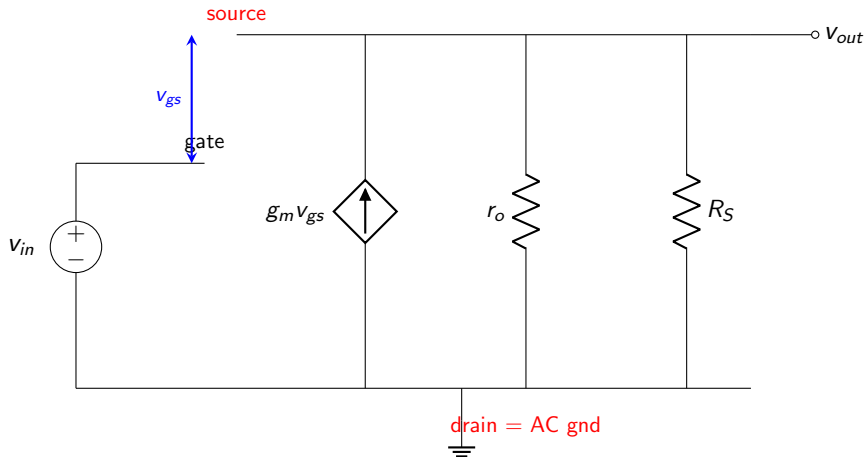
No r_{π} : Gate draws zero current (infinite input impedance).

Small-Signal Step 2: Small-Signal Model



Simpler than BJT: no r_{π} (gate is open circuit). Only $g_m v_{gs}$, r_o , and R_S .

Small-Signal Step 3: Rearranged Model



$g_m v_{gs}$, r_o , and R_S are all in parallel between v_{out} and ground.
Gate is open — v_{in} sets v_{gs} directly (no current through gate).

Voltage Gain Derivation

From the circuit: $v_{gs} = v_{in} - v_{out}$

KCL at v_{out} (ignoring r_o): current from $g_m v_{gs}$ flows through R_S :

$$g_m v_{gs} = \frac{v_{out}}{R_S}$$

Replace $v_{gs} = v_{in} - v_{out}$:

$$g_m (v_{in} - v_{out}) = \frac{v_{out}}{R_S}$$

Solving for v_{out}/v_{in} :

$$A_v = \frac{g_m R_S}{1 + g_m R_S} \approx 1$$