EE461g: Introduction to Electronic Circuits

Lecture 12

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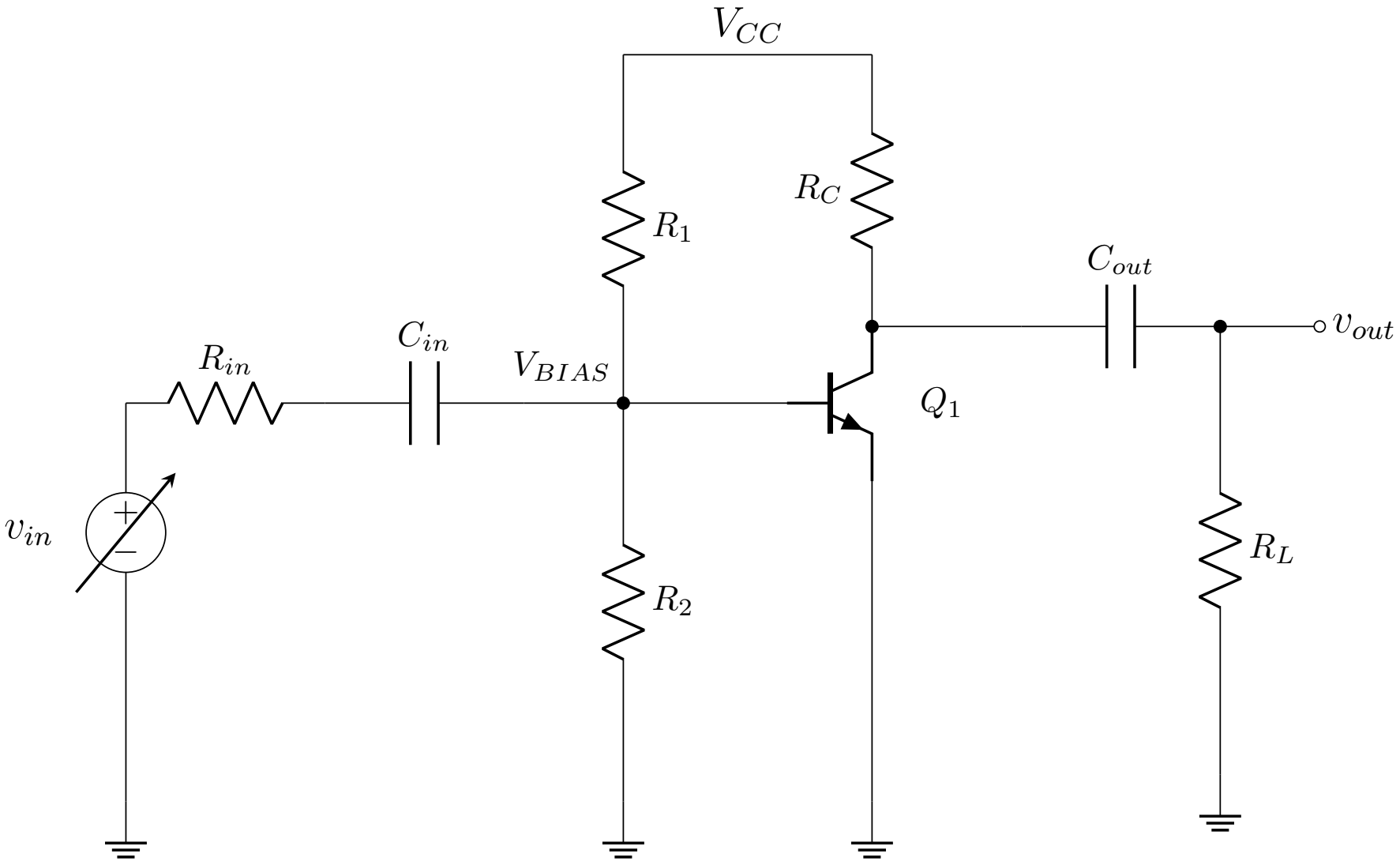
Outline

The CE Amplifier Circuit

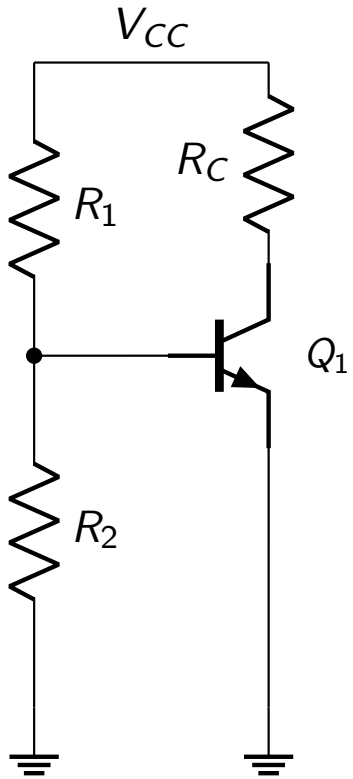
The CE Amplifier with Voltage Divider Bias



CE Large-Signal Analysis (DC Bias)

Capacitors as Open Circuits at DC

- For **DC analysis**, coupling capacitors (C_{in}, C_{out}) are **open circuits**
- Large capacitors block DC current: $I_C = C \cdot dV/dt = 0$ at DC
- This **disconnects** v_{in}, R_{in}, and R_L from the circuit
- Only the bias network (R_1, R_2) and R_C remain



Key idea: At DC, the amplifier reduces to a simple bias circuit

Thévenin Equivalent of the Bias Network

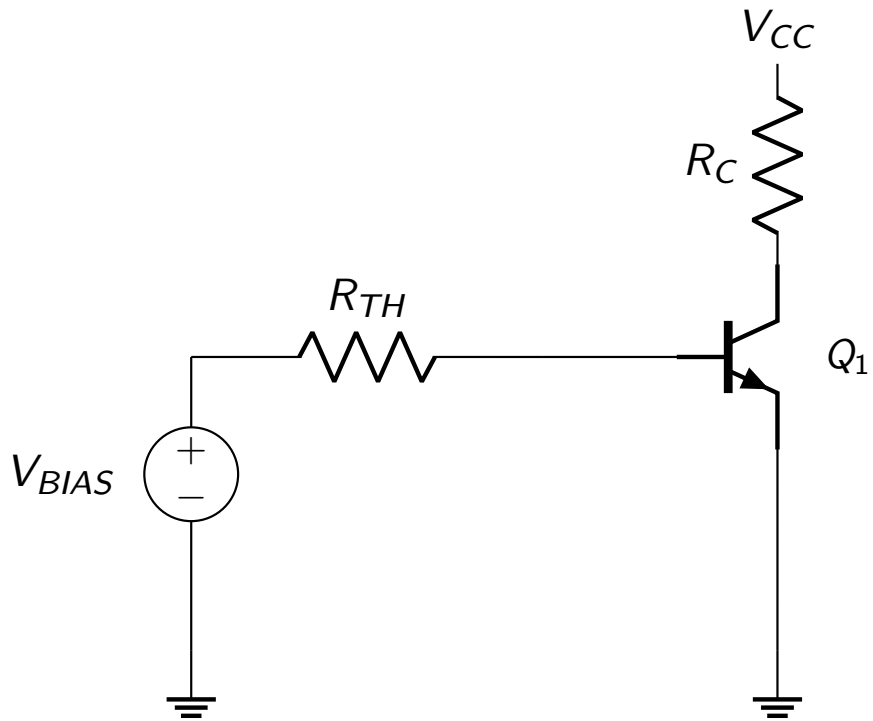
Step 1: Remove Q_1 from the base node.

Step 2: Open-circuit voltage (voltage divider):

$$V_{BIAS} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

Step 3: Short V_{CC}, find resistance:

$$R_{TH} = R_1 \| R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$



Finding the Q-Point

KVL around the base–emitter loop:

$$V_{BIAS} = I_B \cdot R_{TH} + V_{BE}$$

Since $I_C = \beta I_B$, substitute $I_B = I_C/\beta$:

$$V_{BIAS} = \frac{I_C}{\beta} \cdot R_{TH} + V_{BE}$$

Problem: V_{BE} depends on I_C (exponential relationship), so we must solve **iteratively** (as in Lectures 7–8)

Iterative approach:

1. Guess $V_{BE} \approx 0.7$ V $\Rightarrow$ solve for I_C
2. Update V_{BE} using $V_{BE} = V_T \ln(I_C/I_S)$
3. Repeat until V_{BE} converges

Collector–emitter voltage:

$$\boxed{V_{CE} = V_{CC} - I_C \cdot R_C}$$

CE Q-Point Summary

CE Amplifier Q-Point

$$\boxed{I_C = \frac{\beta\,(V_{BIAS} - V_{BE})}{R_{TH}}}$$

$$\boxed{V_{CE} = V_{CC} - I_C \cdot R_C}$$

$$\boxed{V_{BIAS} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}}$$

Verify: $V_{CE} > V_{BE}$ to confirm the transistor is in **forward active** mode

CE Small-Signal Analysis (AC Gain)

Capacitors as Short Circuits at AC

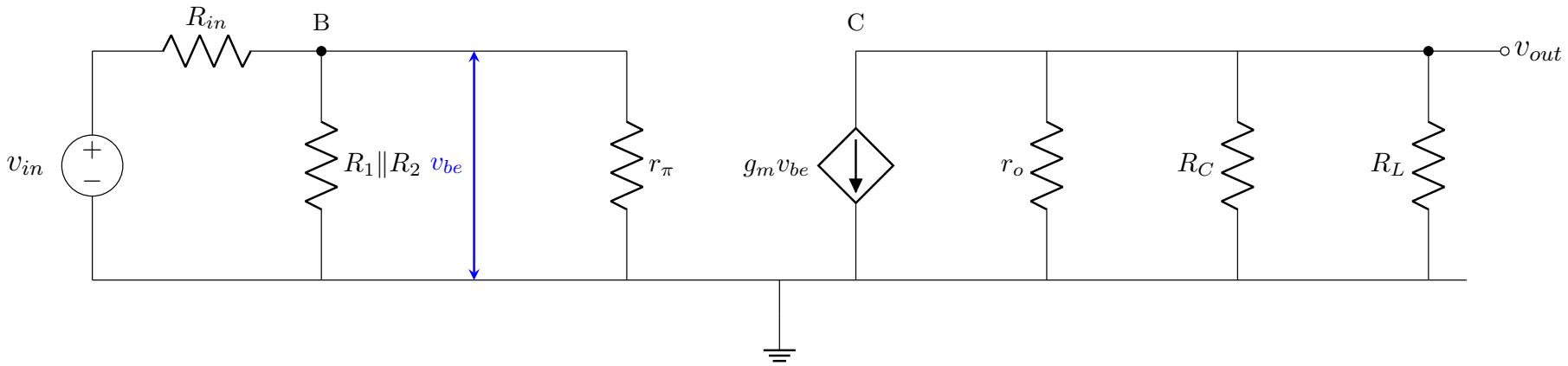
- For **AC small-signal analysis**, coupling capacitors are **short circuits**
- At signal frequencies: $Z_C = 1/(j\omega C) \approx 0$ for large C
- DC voltage sources (V_{CC}) are also **shorted to ground**

Result: C_{in} connects v_{in} directly to the base network; C_{out} connects R_L directly to the collector

Small-signal model parameters (from Q-point):

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_o = \frac{V_A}{I_C}$$

CE Small-Signal Equivalent Circuit



$R_1 \| R_2$ at input, r_π from base to emitter, $g_m v_{be}$ controlled source, $r_o \| R_C \| R_L$ at output

CE Voltage Gain Derivation

Step 1: Input voltage divider determines v_{be}:

$$v_{be} = v_{in} \cdot \frac{R_1 \| R_2 \| r_\pi}{R_{in} + R_1 \| R_2 \| r_\pi}$$

Step 2: Output voltage from controlled source:

$$v_{out} = -g_m \, v_{be} \cdot (r_o \| R_C \| R_L)$$

Step 3: Overall voltage gain:

$$\boxed{A_v = \frac{v_{out}}{v_{in}} = -g_m \cdot \frac{R_1 \| R_2 \| r_\pi}{R_{in} + R_1 \| R_2 \| r_\pi} \cdot (r_o \| R_C \| R_L)}$$

Negative sign $\Rightarrow$ CE amplifier is **inverting**

CE Gain — Simplified

If $R_1 \| R_2 \gg r_\pi$ (typical for well-designed bias):

$$R_1 \| R_2 \| r_\pi \approx r_\pi$$

Simplified voltage gain:

$$\boxed{A_v \approx -g_m \cdot \frac{r_\pi}{R_{in} + r_\pi} \cdot (R_C \| R_L)}$$

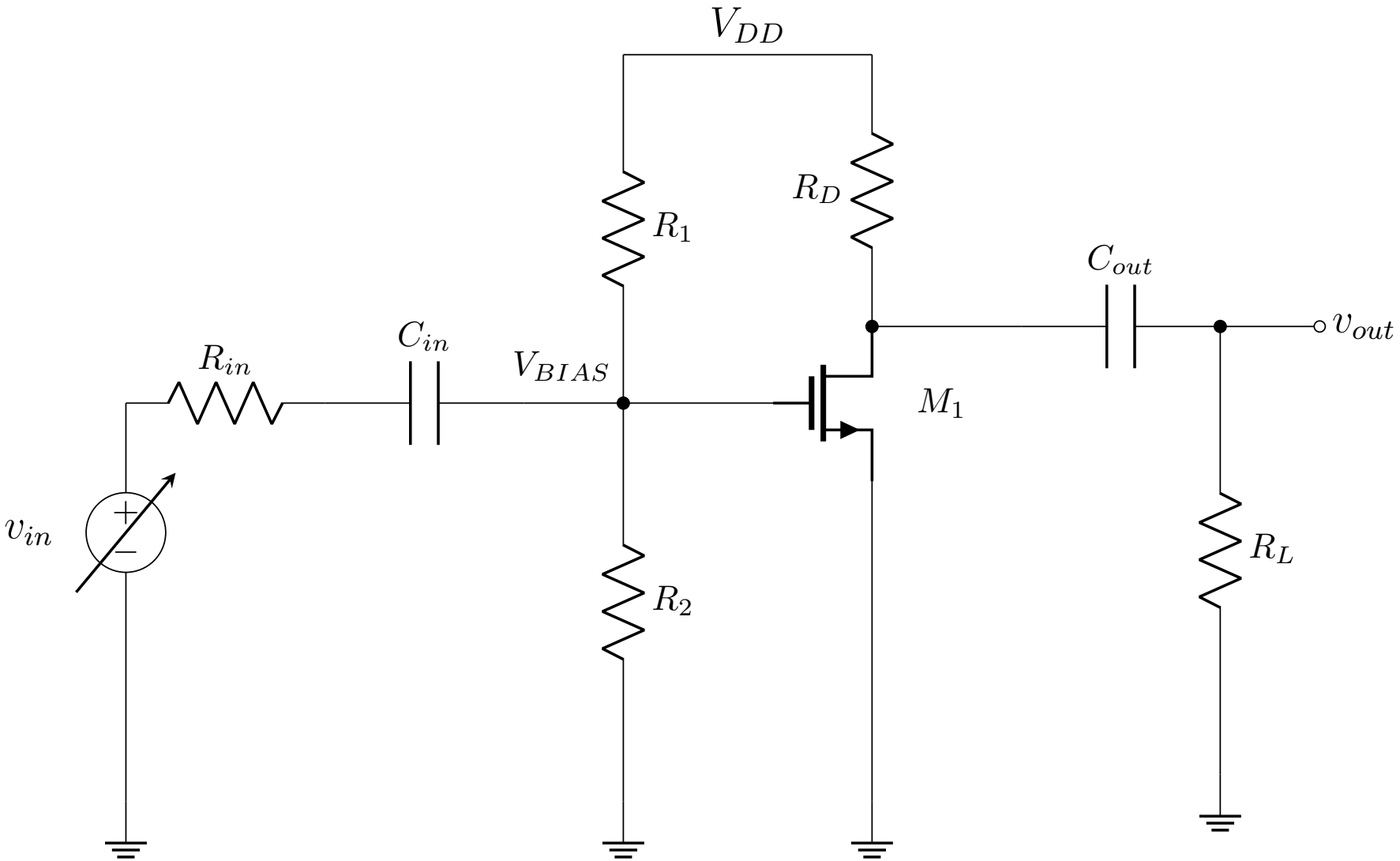
If additionally $r_o \gg R_C \| R_L$ (often true):

$$r_o \| R_C \| R_L \approx R_C \| R_L$$

The gain is set by g_m, the input voltage divider (r_π vs R_{in}), and the output parallel resistance ($R_C \| R_L$)

The CS Amplifier Circuit

The CS Amplifier with Voltage Divider Bias

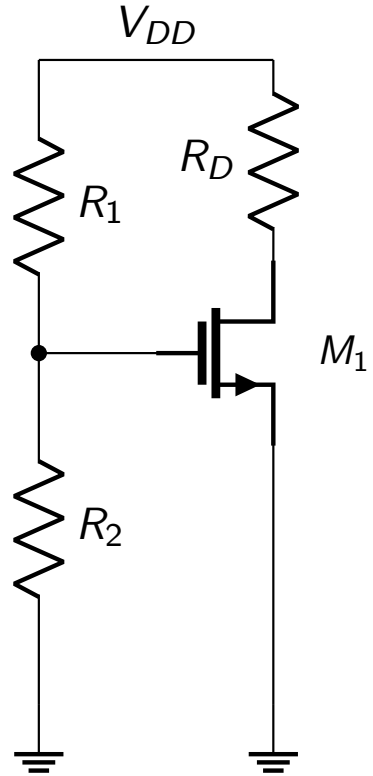


CS Large-Signal Analysis (DC Bias)

Capacitors as Open Circuits at DC

- Same principle: C_{in} and C_{out} are open circuits at DC
- Disconnects v_{in}, R_{in}, and R_L
- Only bias network (R_1, R_2) and R_D remain

Key difference: $I_G = 0$ for a MOSFET, so R_{TH} has **no effect** on the gate voltage!



Thévenin Equivalent of the Bias Network

Same Thévenin procedure:

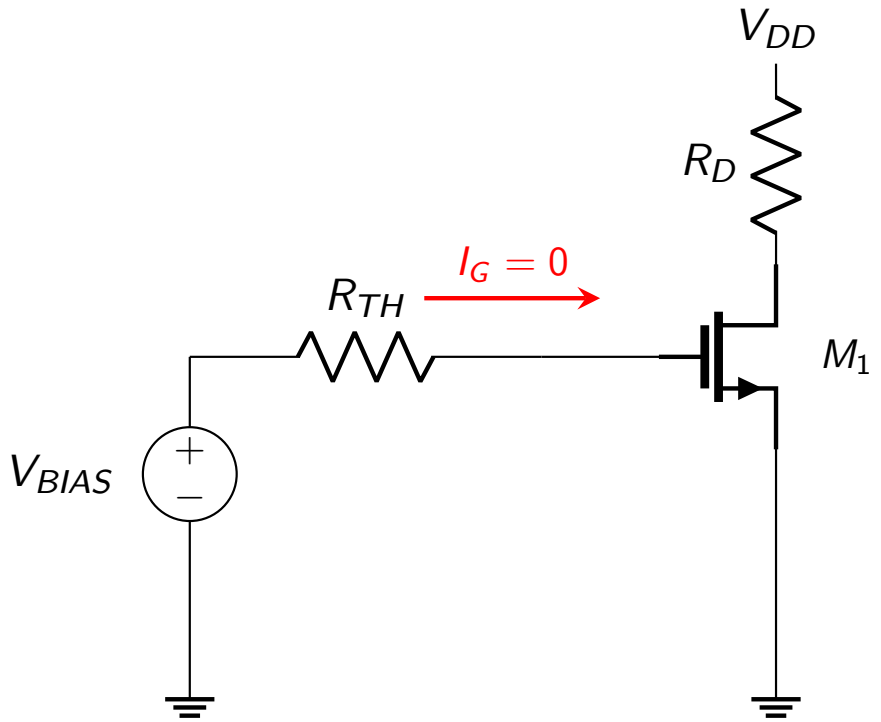
$$V_{BIAS} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

$$R_{TH} = R_1 \| R_2$$

Since $I_G = 0$:

$$V_{GS} = V_{BIAS} - I_G \cdot R_{TH} = V_{BIAS}$$

No voltage drop across R_{TH}!



Finding the Q-Point

Since $I_G = 0$:

$$\boxed{V_{GS} = V_{BIAS} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}}$$

Drain current (saturation region):

$$\boxed{I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2}$$

Drain–source voltage:

$$\boxed{V_{DS} = V_{DD} - I_{DS} \cdot R_D}$$

No iteration needed! Unlike the BJT, V_{GS} is known directly from the voltage divider. Just plug in and solve.

CS Q-Point Summary

CS Amplifier Q-Point

$$\boxed{V_{GS} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}}$$

$$\boxed{I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2}$$

$$\boxed{V_{DS} = V_{DD} - I_{DS} \cdot R_D}$$

Verify: $V_{DS} > V_{GS} - V_{TN}$ to confirm the MOSFET is in **saturation**

CS Small-Signal Analysis (AC Gain)

Capacitors as Short Circuits at AC

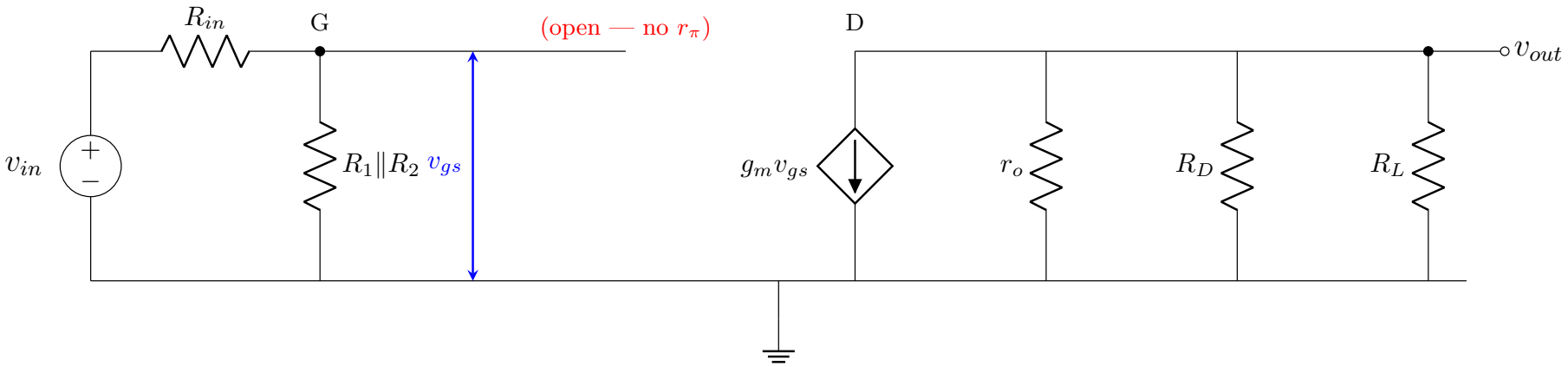
- Same principle as BJT case: capacitors become short circuits at AC
- DC source V_{DD} is shorted to ground
- C_{in} connects v_{in} directly to the gate network
- C_{out} connects R_L directly to the drain

Small-signal model parameters (from Q-point):

$$\boxed{g_m = K_n (V_{GS} - V_{TN})} \qquad \boxed{r_o = \frac{1}{\lambda I_{DS}}}$$

No r_π! The MOSFET gate draws zero current $\Rightarrow$ infinite input impedance

CS Small-Signal Equivalent Circuit



$R_1 \| R_2$ at input, gate is open (no r_π), $g_m v_{gs}$ controlled source, $r_o \| R_D \| R_L$ at output

CS Voltage Gain Derivation

Step 1: Input voltage divider determines v_{gs}:

$$v_{gs} = v_{in} \cdot \frac{R_1 \| R_2}{R_{in} + R_1 \| R_2}$$

No r_π in parallel! The gate is an open circuit, so only $R_1 \| R_2$ loads the input.

Step 2: Output voltage:

$$v_{out} = -g_m \, v_{gs} \cdot (r_o \| R_D \| R_L)$$

Step 3: Overall voltage gain:

$$\boxed{A_v = \frac{v_{out}}{v_{in}} = -g_m \cdot \frac{R_1 \| R_2}{R_{in} + R_1 \| R_2} \cdot (r_o \| R_D \| R_L)}$$

CS Gain Summary

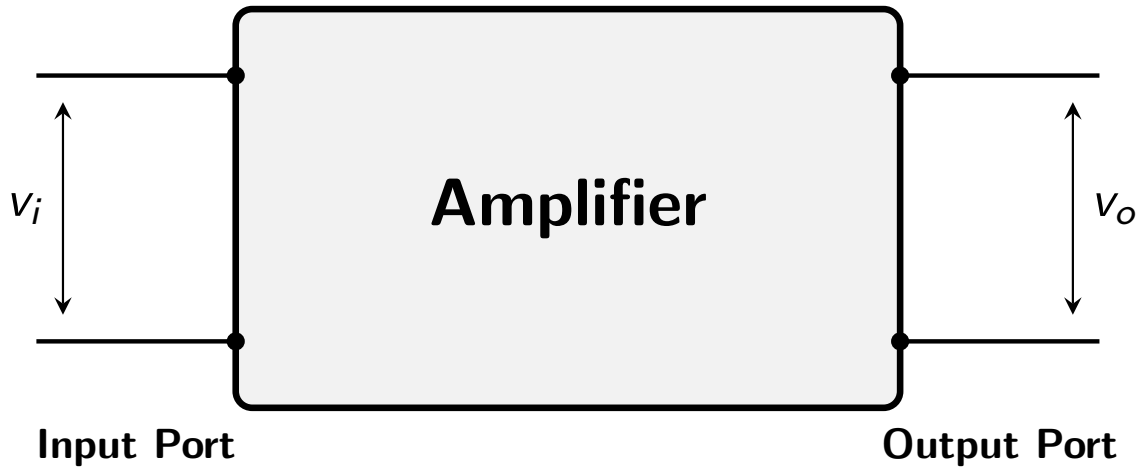
CS Amplifier Voltage Gain

$$A_v = -g_m \cdot \frac{R_1 \| R_2}{R_{in} + R_1 \| R_2} \cdot (r_o \| R_D \| R_L)$$

- **Simpler** than the BJT CE gain — no r_π term in the input divider
- Infinite gate impedance means $R_1 \| R_2$ can be made very large without loss
- Still **inverting** (negative sign)

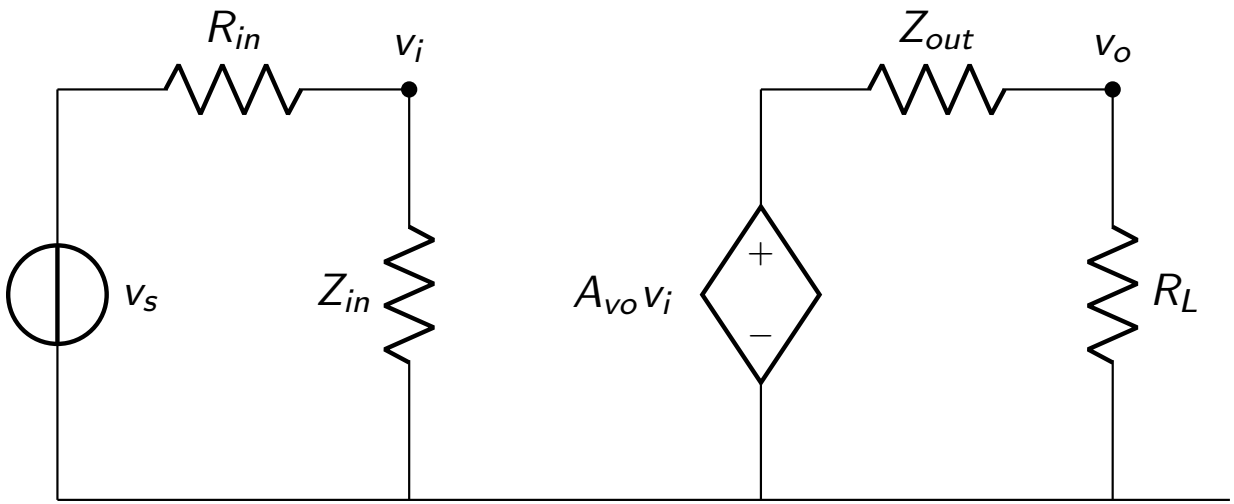
Two-Port Network Model

What is a Two-Port Network?



- A **two-port network** is a "black box" with an input port and an output port
- For a **voltage amplifier**, fully characterized by three parameters:
  1. **Input impedance** Z_{in}: resistance looking into the input
  2. **Output impedance** Z_{out}: resistance looking back into the output
  3. **Open-circuit voltage gain** A_{vo}: gain when $R_L = \infty$
- Our small-signal amplifier models *are* two-port networks

Voltage Amplifier Two-Port Equivalent



The overall voltage gain is a product of **three factors**:

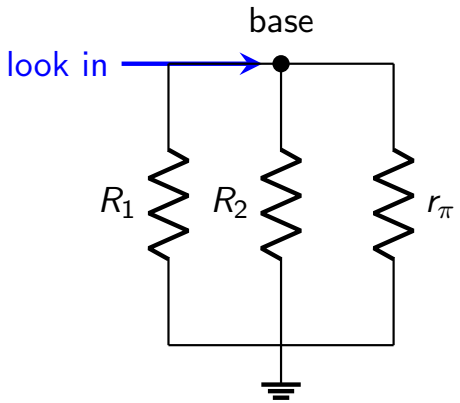
$$A_v = \frac{v_o}{v_s} = \underbrace{\frac{Z_{in}}{R_{in} + Z_{in}}}_{\text{input divider}} \cdot A_{vo} \cdot \underbrace{\frac{R_L}{Z_{out} + R_L}}_{\text{output divider}}$$

Once you know Z_{in}, Z_{out}, and A_{vo}, you can find the gain for **any** source and load

Deriving the Input Impedance Z_{in}

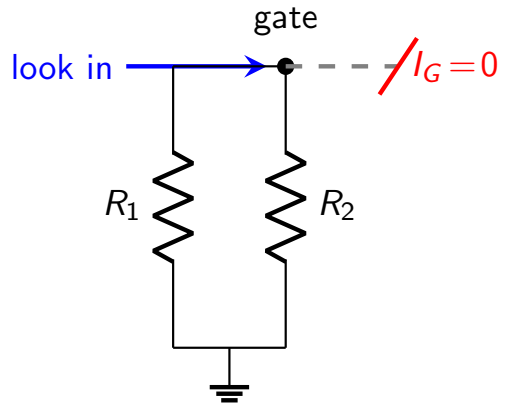
Method: Disconnect the source. Look into the input port of the small-signal circuit.
DC supplies are **AC ground**; capacitors are **short circuits**.

CE (BJT)



$$Z_{in} = R_1 \| R_2 \| r_\pi$$

CS (MOSFET)



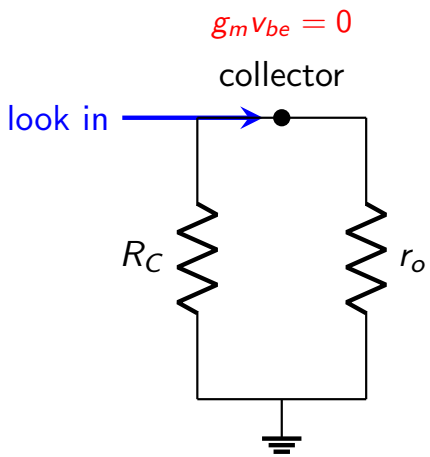
$$Z_{in} = R_1 \| R_2$$

The MOSFET's infinite gate impedance means r_π does **not** load the input $\Rightarrow$ CS has higher Z_{in} than CE

Deriving Z_{out} and A_{vo}

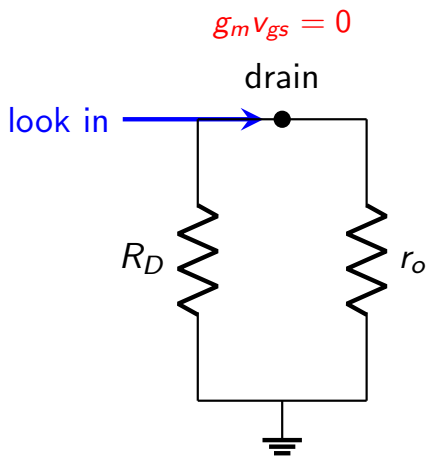
Z_{out}: Zero the input ($v_{be} = 0$ or $v_{gs} = 0$), so $g_m \cdot 0 = 0$ — controlled source turns off.
Look back into the output port.

CE (BJT)



$$Z_{out} = r_o \| R_C$$

CS (MOSFET)



$$Z_{out} = r_o \| R_D$$

A_{vo} **(open-circuit gain):** Set $R_L = \infty$. Since $v_{be} = v_i$ (or $v_{gs} = v_i$):

$$v_o = -g_m v_i \cdot Z_{out} \quad \Rightarrow \quad \boxed{A_{vo} = -g_m \cdot Z_{out}}$$

CE and CS Two-Port Parameters

Parameter	CE (BJT)	CS (MOSFET)
Z_{in}	$R_1 \| R_2 \| r_\pi$	$R_1 \| R_2$
Z_{out}	$r_o \| R_C$	$r_o \| R_D$
A_{vo}	$-g_m (r_o \| R_C)$	$-g_m (r_o \| R_D)$

Key difference: The MOSFET gate draws no current $\Rightarrow$ no r_π loading the input

CS amplifier has **higher input impedance** than CE

Finding Z_{out}: Zero the input ($v_{be} = 0$ or $v_{gs} = 0$), short DC supplies to ground,
and find the resistance looking back into the output node

BJT vs MOSFET Comparison

CE vs CS Amplifier — Side-by-Side

Property	**BJT (CE)**	**MOSFET (CS)**
Bias voltage	$V_{BIAS} = V_{CC}\frac{R_2}{R_1+R_2}$	$V_{BIAS} = V_{DD}\frac{R_2}{R_1+R_2}$
Effect of R_{TH}	Drops voltage ($I_B \neq 0$)	No effect ($I_G = 0$)
Q-point method	Iterative (exponential)	Direct (square-law)
Input impedance	$R_1 \| R_2 \| r_\pi$	$R_1 \| R_2$ (infinite gate)
Input divider	$\frac{R_1 \| R_2 \| r_\pi}{R_{in} + R_1 \| R_2 \| r_\pi}$	$\frac{R_1 \| R_2}{R_{in} + R_1 \| R_2}$
Gain	$-g_m \cdot (\text{div}) \cdot (r_o \| R_C \| R_L)$	$-g_m \cdot (\text{div}) \cdot (r_o \| R_D \| R_L)$

Same structure, but the MOSFET's infinite gate impedance simplifies both bias and gain analysis

SPICE Verification

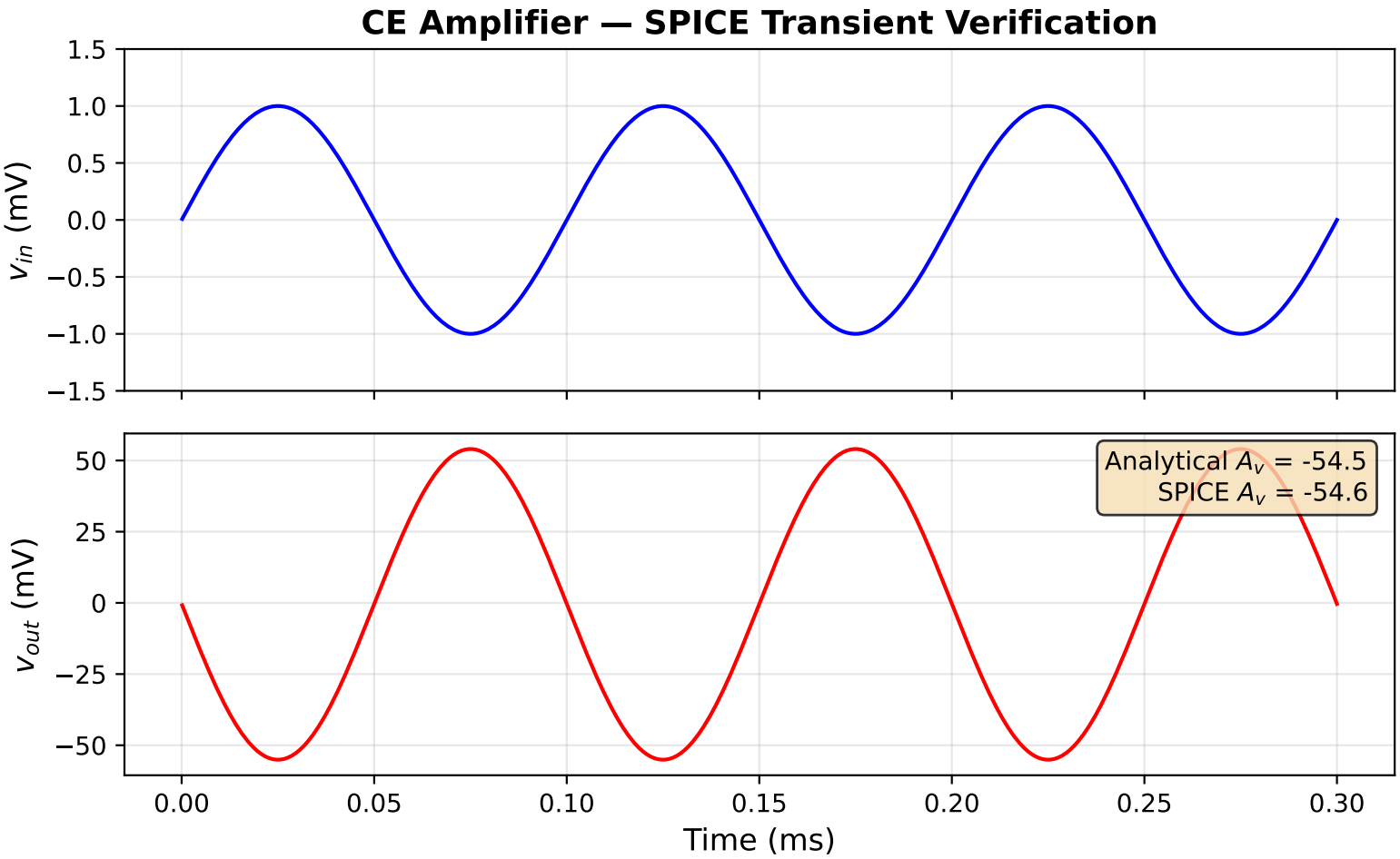
CE SPICE Verification — Q-Point

```
* CE Amplifier - Operating Point
.options TEMP=28.42 TNOM=28.42
VCC vcc 0 DC 10
R1 vcc base 200k
R2 base 0 100k
Q1 col base 0 NPN1
RC vcc col 1k
.model NPN1 NPN(IS=1e-14
+  BF=100)
.end
```

	Analytical	**SPICE**	
I_C	3.96 mA	3.96 mA	✓
V_{BE}	0.694 V	0.694 V	✓
V_{CE}	6.04 V	6.04 V	✓

SPICE confirms our iterative Q-point solution — values match exactly

CE SPICE Verification — Voltage Gain



	Analytical	**SPICE**
A_v	-54.6	-54.6

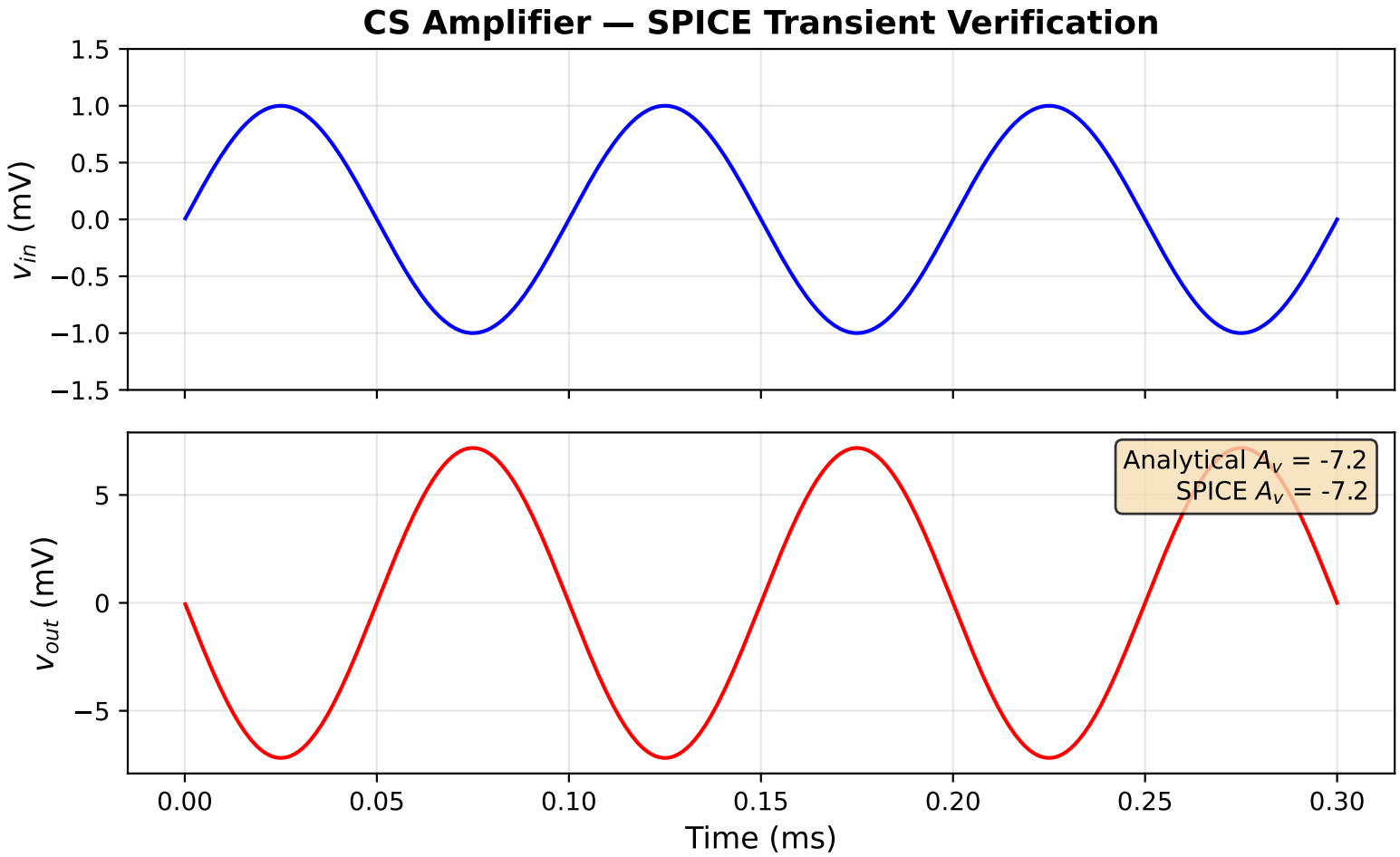
CS SPICE Verification — Q-Point

```
* CS Amplifier - Operating Point
VDD vdd 0 DC 10
R1 vdd gate 400k
R2 gate 0 100k
M1 drain gate 0 0 NMOS1
+  W=1u L=1u
RD vdd drain 1k
.model NMOS1 NMOS(KP=8m
+  VTO=1 LAMBDA=0)
.end
```

	Analytical	**SPICE**	
I_{DS}	4.00 mA	4.00 mA	✓
V_{GS}	2.00 V	2.00 V	✓
V_{DS}	6.00 V	6.00 V	✓

SPICE confirms the direct Q-point calculation — values match exactly

CS SPICE Verification — Voltage Gain



	Analytical	**SPICE**
A_v	-7.2	-7.2

SPICE Verification — Summary

All analytical results confirmed by SPICE — exact match for Q-point and gain

Numerical Two-Port Parameters from SPICE Circuits

Parameter	CE (BJT)	CS (MOSFET)
g_m	152.4 mA/V	8.0 mA/V
r_π	657 Ω	∞
r_o	∞ (no V_A)	∞ ($\lambda = 0$)
Z_{in}	$R_1 \| R_2 \| r_\pi = 650$ Ω	$R_1 \| R_2 = 80$ kΩ
Z_{out}	$r_o \| R_C = 1.00$ kΩ	$r_o \| R_D = 1.00$ kΩ
A_{vo}	-152.4	-8.0
A_v	-54.6	-7.2

CE has much higher g_m (and $|A_{vo}|$), but its low Z_{in} causes significant input signal loss