EE461g: Introduction to Electronic Circuits

Lecture 14

Dr. Lau

University of Kentucky

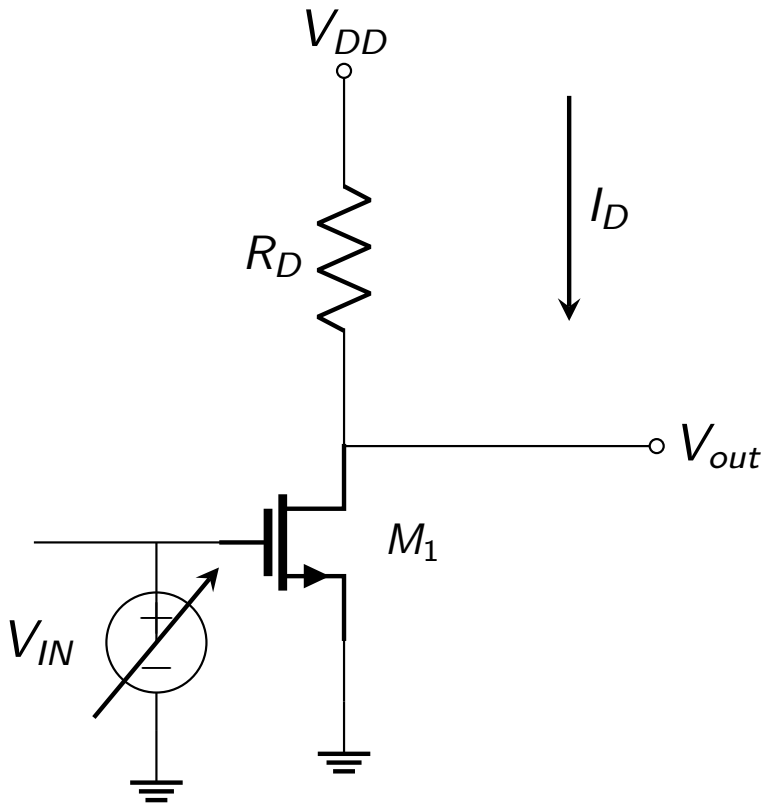
Outline

Three Ways to Load a CS Amplifier

CS with Resistor Load

(Review from Lecture 10)

CS Amplifier with Resistor Load



Resistor R_D connects drain to V_{DD}. Simple, but R_D is **passive** — does not depend on V_{IN}.

$$V_{DD} = 10 \text{ V}, \quad K_n = 10 \text{ mA/V}^2, \quad V_{TN} = 0.7 \text{ V}, \quad \lambda = 0, \quad R_D = 1 \text{ k}\Omega$$

Resistor Load: VTC Equations

M_1 in saturation ($V_{DS} \geq V_{GS} - V_{TN}$):

$$I_D = \frac{K_n}{2}(V_{IN} - V_{TN})^2$$

KVL: $V_{out} = V_{DD} - I_D R_D$

$$\boxed{V_{out} = V_{DD} - \frac{K_n R_D}{2}(V_{IN} - V_{TN})^2}$$

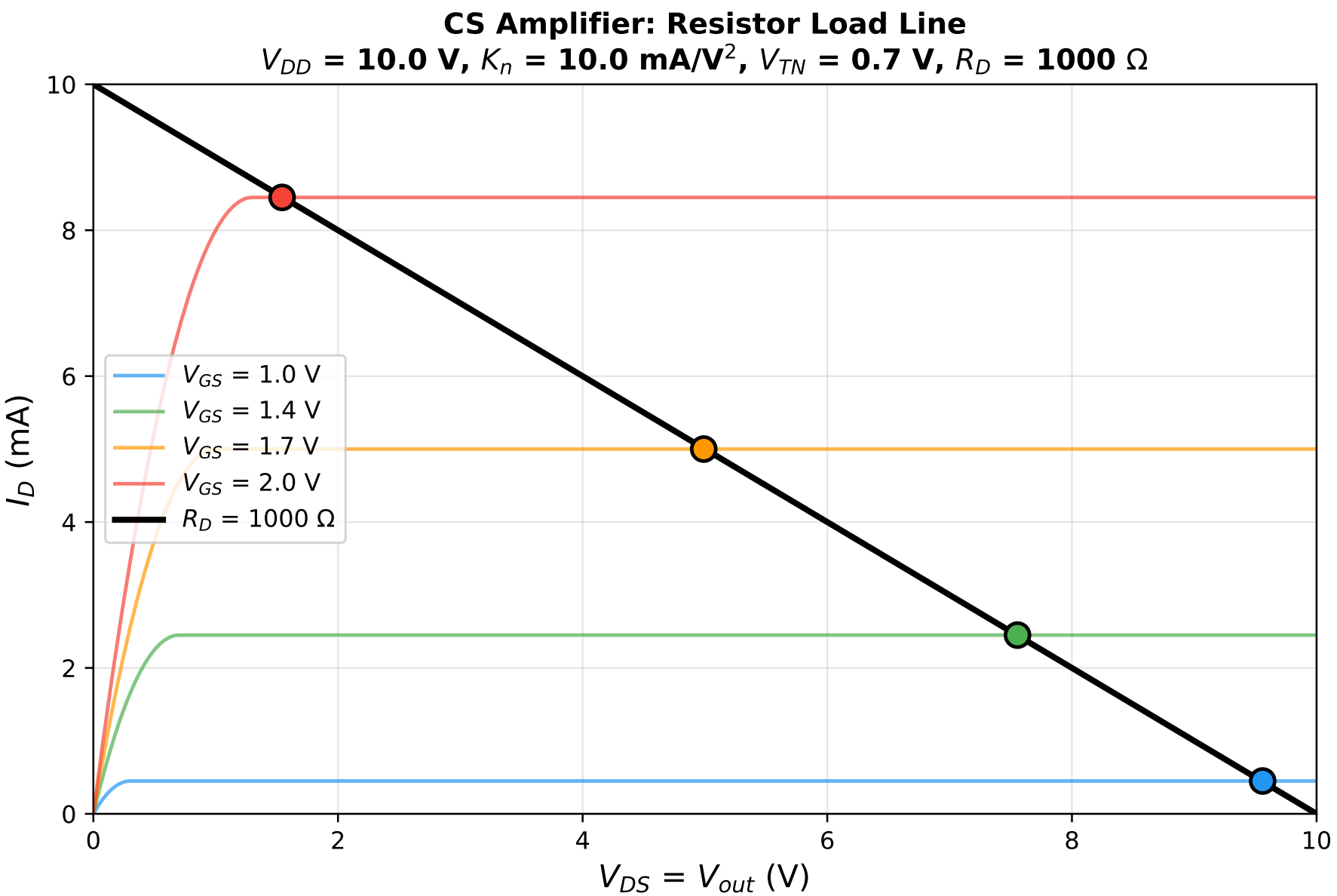
Small-signal gain: $g_m = K_n(V_{IN} - V_{TN})$

$$A_v = -g_m R_D = -K_n(V_{IN} - V_{TN})R_D$$

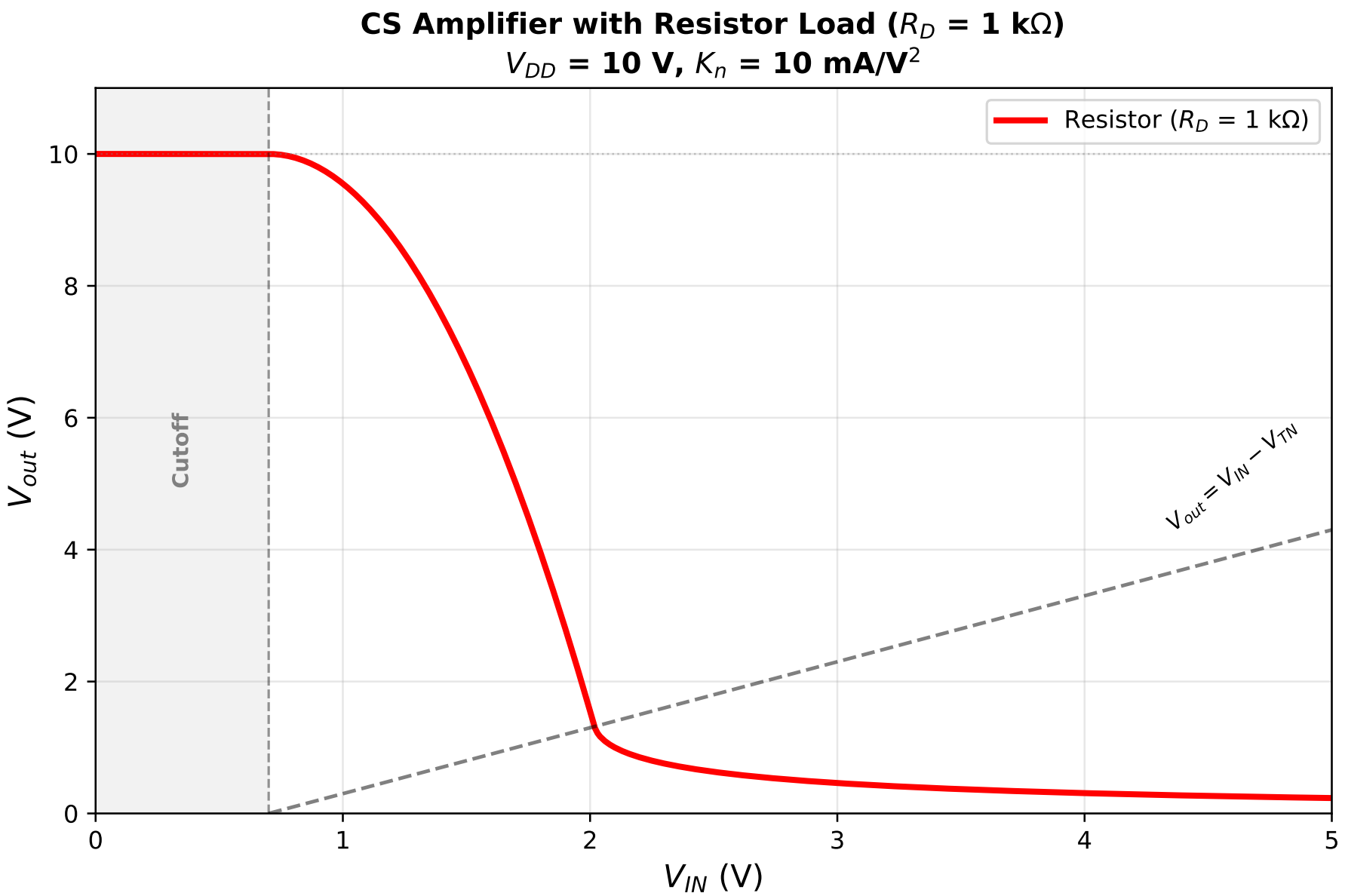
At $V_{IN} = 1.7$ V: $A_v = -10 \times 10^{-3} \times 1.0 \times 1000 = -10$

Note: Gain depends on the operating point (V_{IN}).

Resistor Load: Load Line



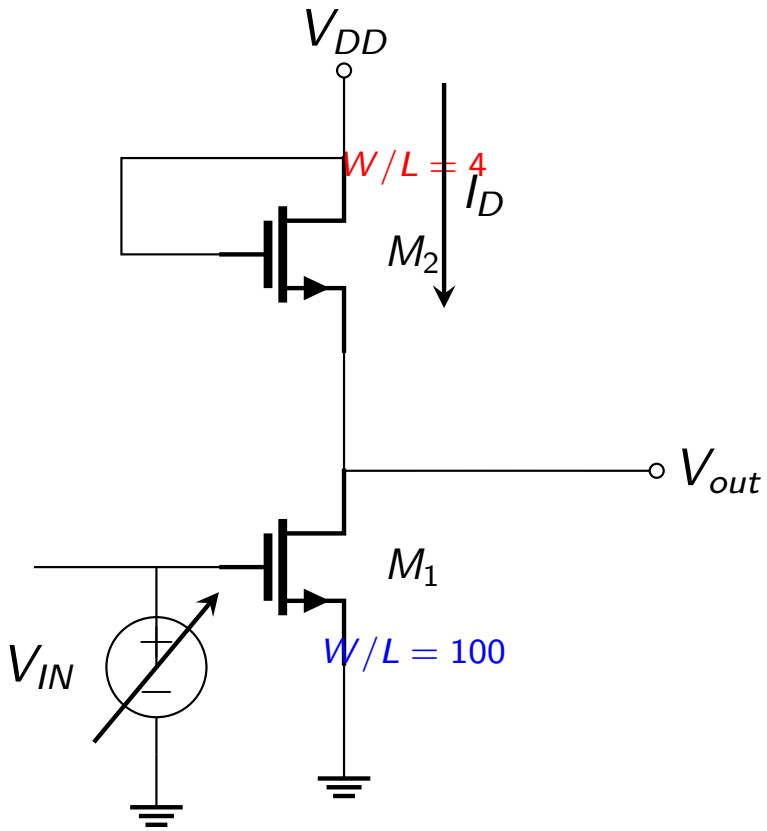
Resistor Load: Transfer Curve



CS with NMOS Active Load

(Review from Lecture 11)

CS Amplifier with Diode-Connected NMOS Load



R_D replaced by diode-connected M_2 (gate tied to drain). Load is **nonlinear** but still does not depend on V_{IN}.

$V_{DD} = 10$ V, $K_{n1} = 10$ mA/V^2, $K_{n2} = 0.4$ mA/V^2, $V_{TN} = 0.7$ V, $\lambda = 0$

NMOS Active Load: VTC Equations

KCL: $I_{D1} = I_{D2}$

M_1 in saturation: $I_{D1} = \frac{K_{n1}}{2}(V_{IN} - V_{TN})^2$

M_2 diode-connected ($V_{GS2} = V_{DD} - V_{out}$):
$I_{D2} = \frac{K_{n2}}{2}(V_{DD} - V_{out} - V_{TN})^2$

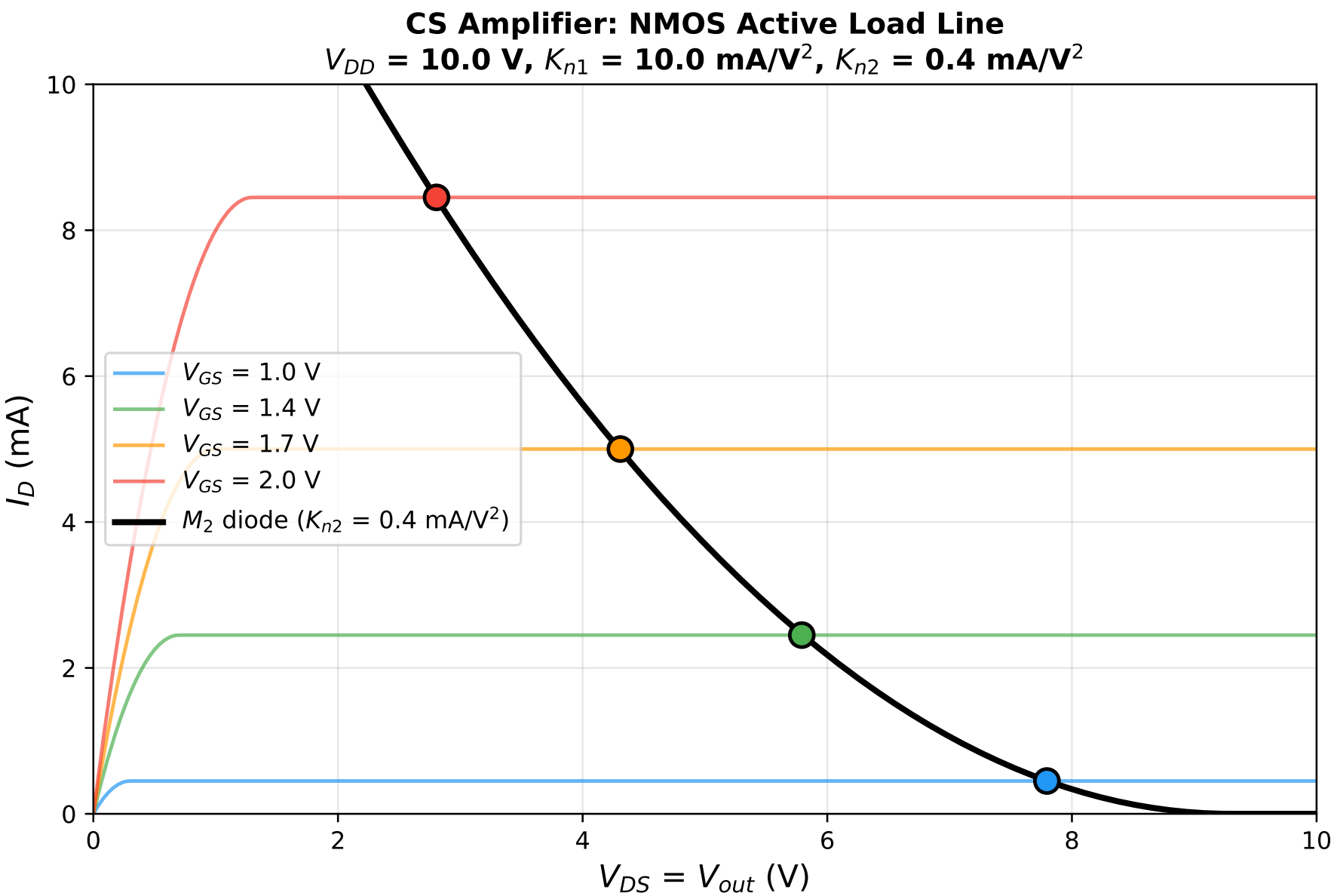
Setting equal and solving:

$$V_{out} = V_{DD} - V_{TN} - \sqrt{\frac{K_{n1}}{K_{n2}}}(V_{IN} - V_{TN})$$

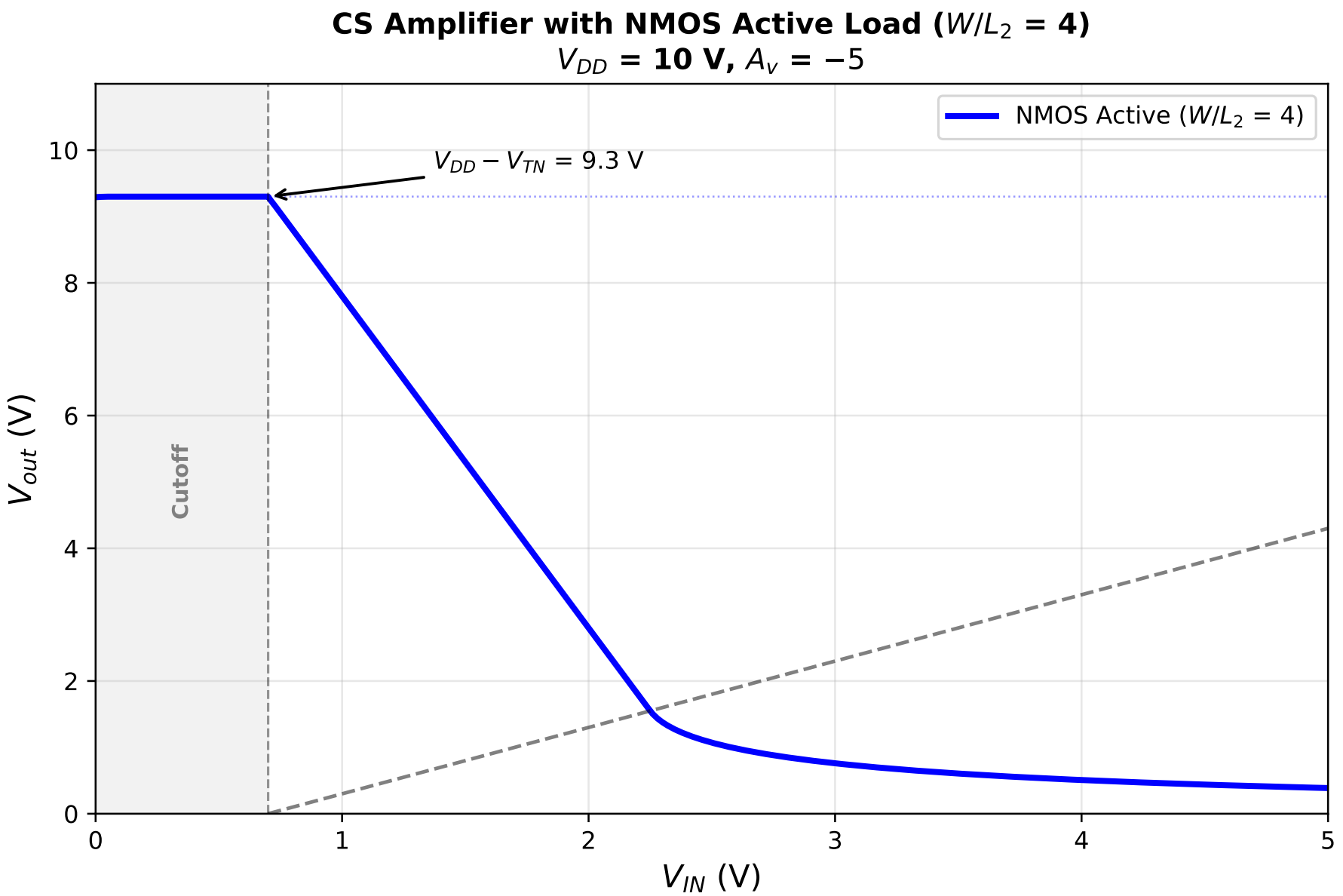
Gain: $A_v = -\sqrt{K_{n1}/K_{n2}} = -\sqrt{25} = -5$

Note: Gain is **constant** in the saturation region — set by W/L ratio.

NMOS Active Load: Load Line



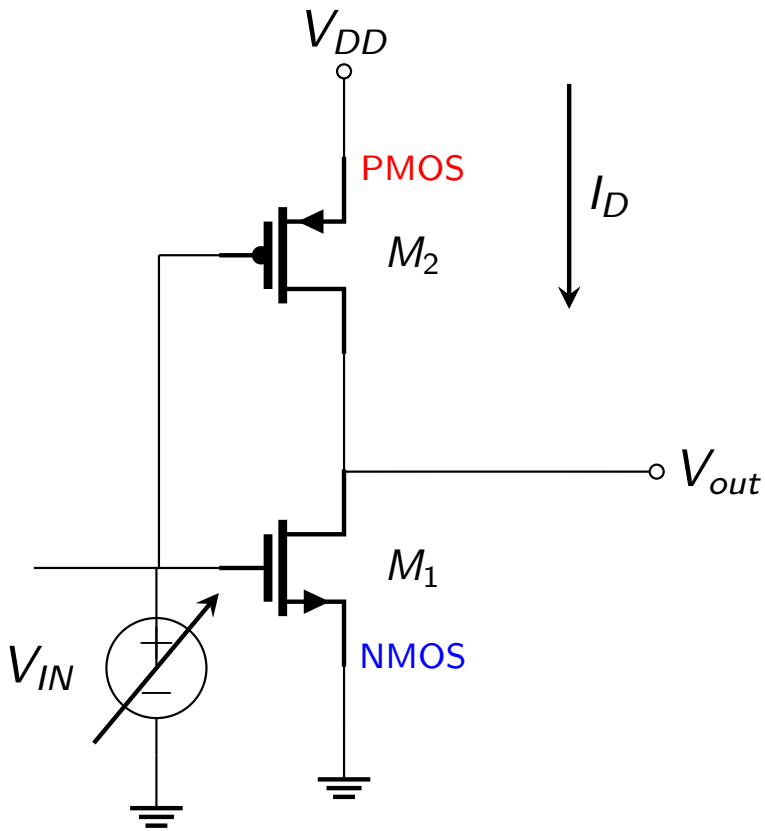
NMOS Active Load: Transfer Curve



CMOS Inverter

Complementary NMOS + PMOS Pair

CMOS Inverter Circuit



M_1 (NMOS) and M_2 (PMOS) share the same gate (V_{IN}) and drain (V_{out}). **Both transistors respond to V_{IN}!**

$$V_{DD} = 10 \text{ V}, \quad K_n = K_p = 10 \text{ mA/V}^2, \quad V_{TN} = |V_{TP}| = 0.7 \text{ V}, \quad \lambda = 0$$

PMOS Current Equation

For the PMOS transistor M_2:

$$I_D = \frac{K_p}{2}(V_{SG} - |V_{TP}|)^2$$

Since $V_S = V_{DD}$ and $V_G = V_{IN}$:

$$V_{SG} = V_{DD} - V_{IN}$$

$$\boxed{I_{D,\text{PMOS}} = \frac{K_p}{2}(V_{DD} - V_{IN} - |V_{TP}|)^2}$$

Key insight: Unlike R_D or diode-connected M_2, the PMOS load current **depends on** V_{IN}!

Both driver AND load change simultaneously as V_{IN} sweeps.

Five Operating Regions

As V_{IN} sweeps from 0 to V_{DD}:

Region	V_{IN} **range**	M_1 **(NMOS)**	M_2 **(PMOS)**
1	$0 \leq V_{IN} < V_{TN}$	Cutoff	Triode
2	$V_{TN} \leq V_{IN} < V_M$	Saturation	Triode
3	$V_{IN} = V_M$	Saturation	Saturation
4	$V_M < V_{IN} \leq V_{DD} - \lvert V_{TP} \rvert$	Triode	Saturation
5	$V_{DD} - \lvert V_{TP} \rvert < V_{IN} \leq V_{DD}$	Triode	Cutoff

V_M = switching threshold (midpoint voltage where both are in saturation).

Region 3 is the **transition region** — the VTC is nearly vertical here. This is where the gain is highest.

Regions 1 & 5: Cutoff Cases

Region 1: $V_{IN} < V_{TN} = 0.7$ V

M_1 is off ($I_D = 0$), M_2 pulls V_{out} to V_{DD}:

$$\boxed{V_{out} = V_{DD} = 10 \text{ V}}$$

Region 5: $V_{IN} > V_{DD} - |V_{TP}| = 9.3$ V

M_2 is off ($I_D = 0$), M_1 pulls V_{out} to 0:

$$\boxed{V_{out} = 0 \text{ V}}$$

Full rail-to-rail output swing: V_{out} goes from 0 to V_{DD}.

Compare: NMOS active load can only reach $V_{DD} - V_{TN} = 9.3$ V.

Region 2: NMOS Sat / PMOS Triode

$V_{TN} < V_{IN} < V_M$: V_{out} is high, M_1 is in saturation, M_2 is in triode.

M_1 (saturation):

$$I_{D1} = \frac{K_n}{2}(V_{IN} - V_{TN})^2$$

M_2 (triode, $V_{SD} = V_{DD} - V_{out}$):

$$I_{D2} = K_p\left[(V_{DD} - V_{IN} - |V_{TP}|)(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}\right]$$

Setting $I_{D1} = I_{D2}$: implicit equation in $V_{out}(V_{IN})$.

No closed-form solution — must solve numerically or with SPICE.

Region 4: NMOS Triode / PMOS Sat

$V_M < V_{IN} < V_{DD} - |V_{TP}|$: V_{out} is low, M_1 is in triode, M_2 is in saturation.

M_1 (triode):

$$I_{D1} = K_n\left[(V_{IN} - V_{TN})V_{out} - \frac{V_{out}^2}{2}\right]$$

M_2 (saturation):

$$I_{D2} = \frac{K_p}{2}(V_{DD} - V_{IN} - |V_{TP}|)^2$$

Setting $I_{D1} = I_{D2}$: symmetric to Region 2.

Also requires numerical solution.

Regions 2 and 4 are **symmetric** for matched $K_n = K_p$, $V_{TN} = |V_{TP}|$.

Region 3: Both in Saturation (Switching Point)

Both M_1 and M_2 in saturation: $I_{D1} = I_{D2}$:

$$\frac{K_n}{2}(V_{IN} - V_{TN})^2 = \frac{K_p}{2}(V_{DD} - V_{IN} - |V_{TP}|)^2$$

Taking the square root:

$$\sqrt{K_n}(V_{IN} - V_{TN}) = \sqrt{K_p}(V_{DD} - V_{IN} - |V_{TP}|)$$

Solving for $V_{IN} = V_M$:

$$\boxed{V_M = \frac{V_{TN} + \sqrt{K_p/K_n}\,(V_{DD} - |V_{TP}|)}{1 + \sqrt{K_p/K_n}}}$$

For matched transistors ($K_n = K_p$, $V_{TN} = |V_{TP}|$):

$$V_M = \frac{V_{TN} + V_{DD} - |V_{TP}|}{2} = \frac{V_{DD}}{2} = 5\ \text{V}$$

Gain at V_M

With $\lambda = 0$ (ideal): both transistors are in saturation at V_M.

The VTC slope at V_M:

$$\left.\frac{dV_{out}}{dV_{IN}}\right|_{V_M} \rightarrow -\infty$$

With $\lambda = 0$: **gain is infinite!** (vertical VTC)

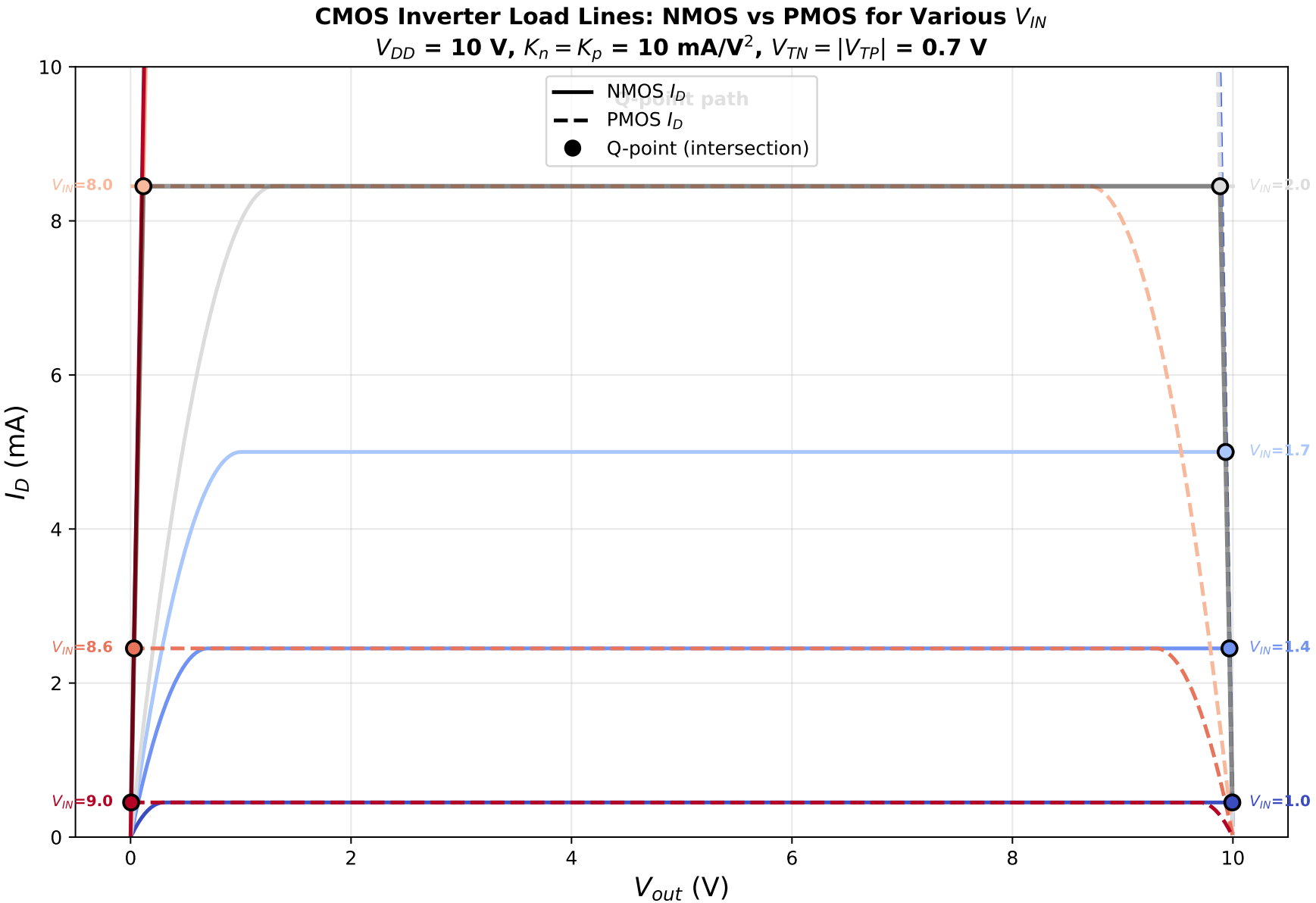
With $\lambda > 0$ (realistic):

$$A_v = -(g_{mn} + g_{mp})(r_{on} \parallel r_{op})$$

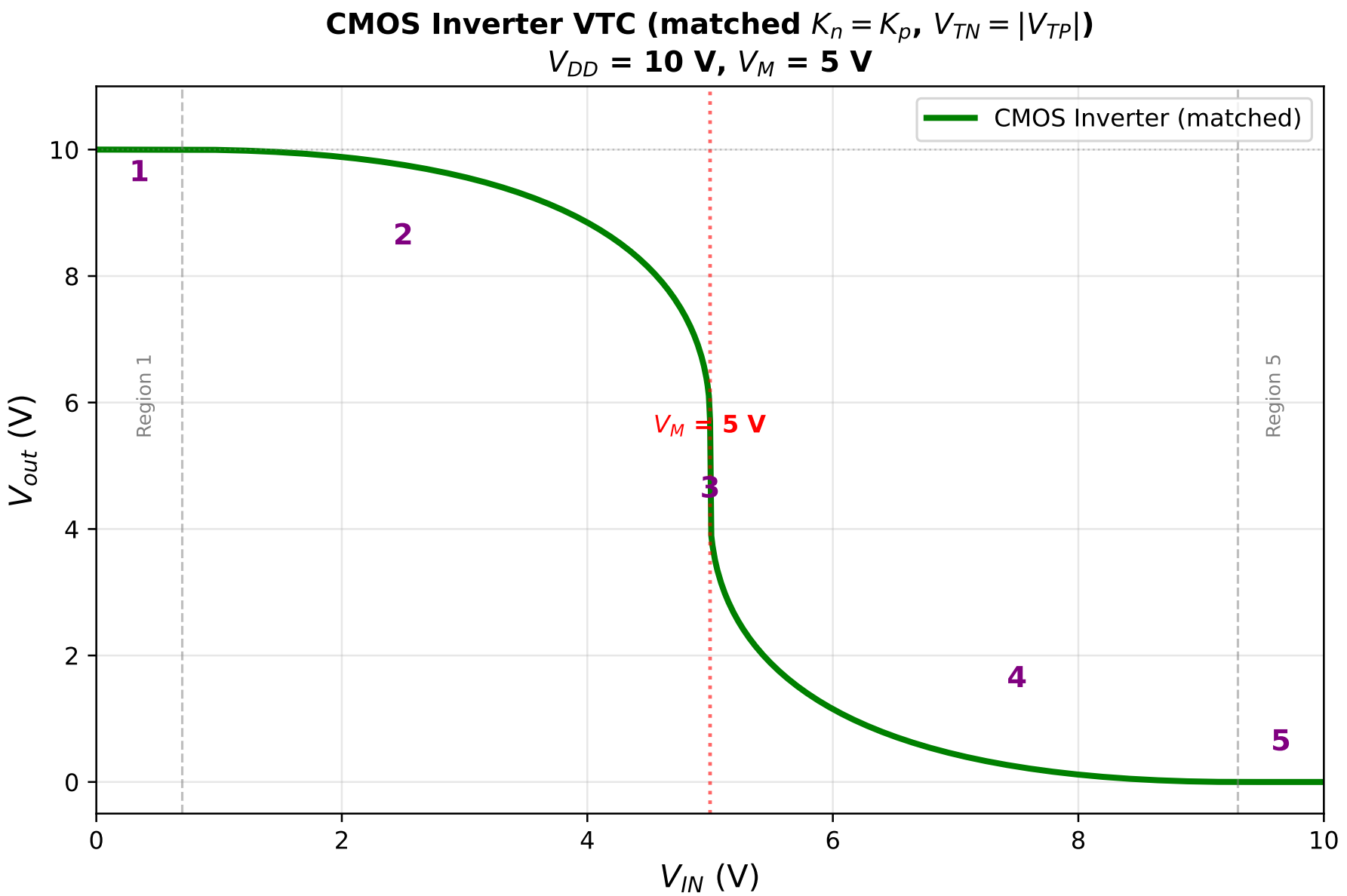
Why so high? Both M_1 and M_2 respond to V_{IN}:

$V_{IN}\uparrow \Rightarrow$ M_1 current $\uparrow$ AND M_2 current $\downarrow$ simultaneously!

CMOS Load Lines



CMOS Inverter: Transfer Curve



Key Insight: Why CMOS Gain Is So High

Load type	**Load current**	**Responds to V_{IN}?**
R_D	$I = \frac{V_{DD} - V_{out}}{R_D}$	No
Diode NMOS	$I = \frac{K_{n2}}{2}(V_{DD} - V_{out} - V_{TN})^2$	No
PMOS	$I = \frac{K_p}{2}(V_{DD} - V_{IN} - \lvert V_{TP} \rvert)^2$	**Yes!**

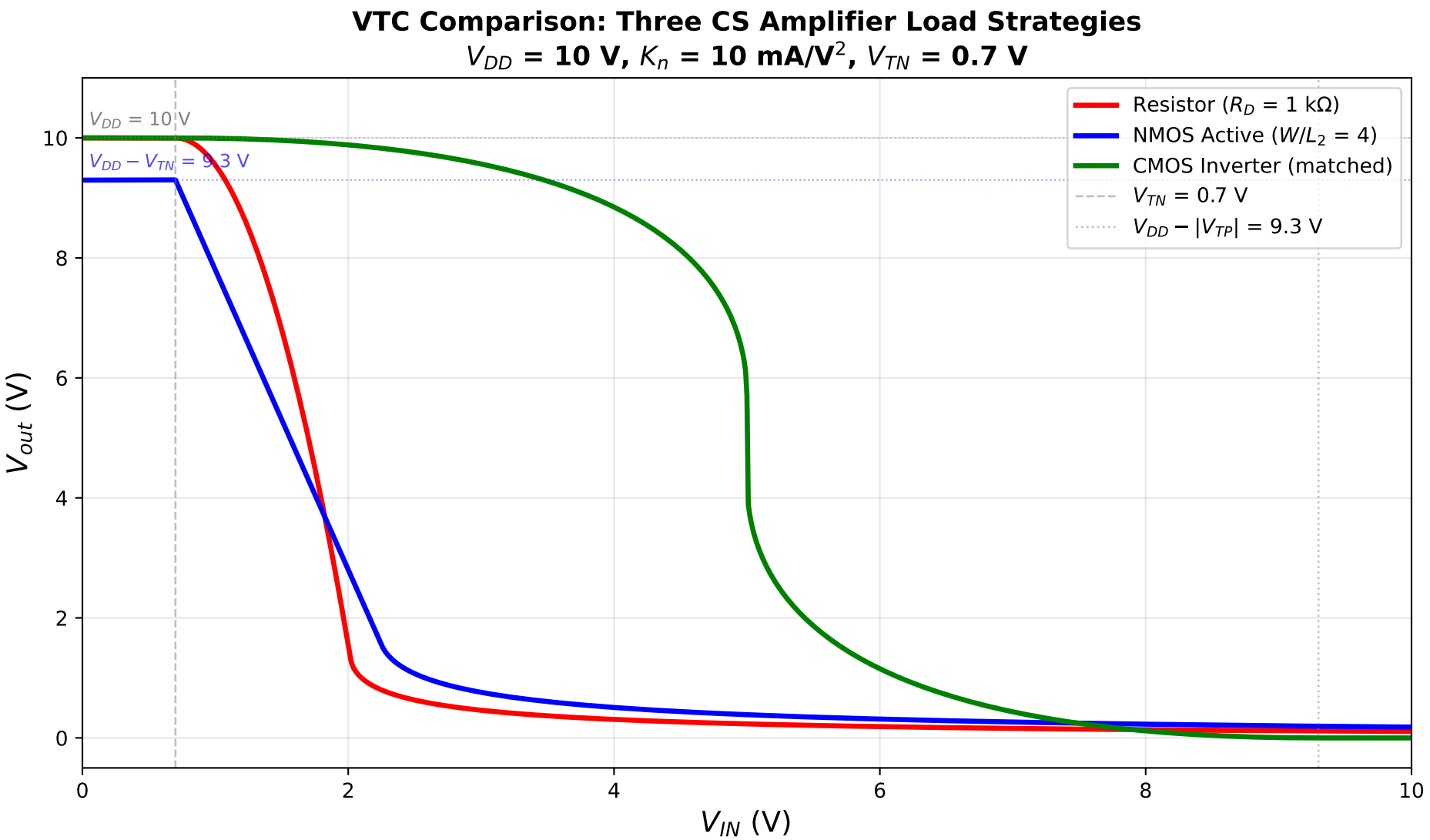
In the CMOS inverter, the load is **not passive**.

When V_{IN} increases: driver (M_1) pushes more current **and** load (M_2) supplies less $\Rightarrow$ V_{out} drops rapidly.

Comparison

Resistor vs NMOS Active vs CMOS

VTC Comparison: All Three Loads



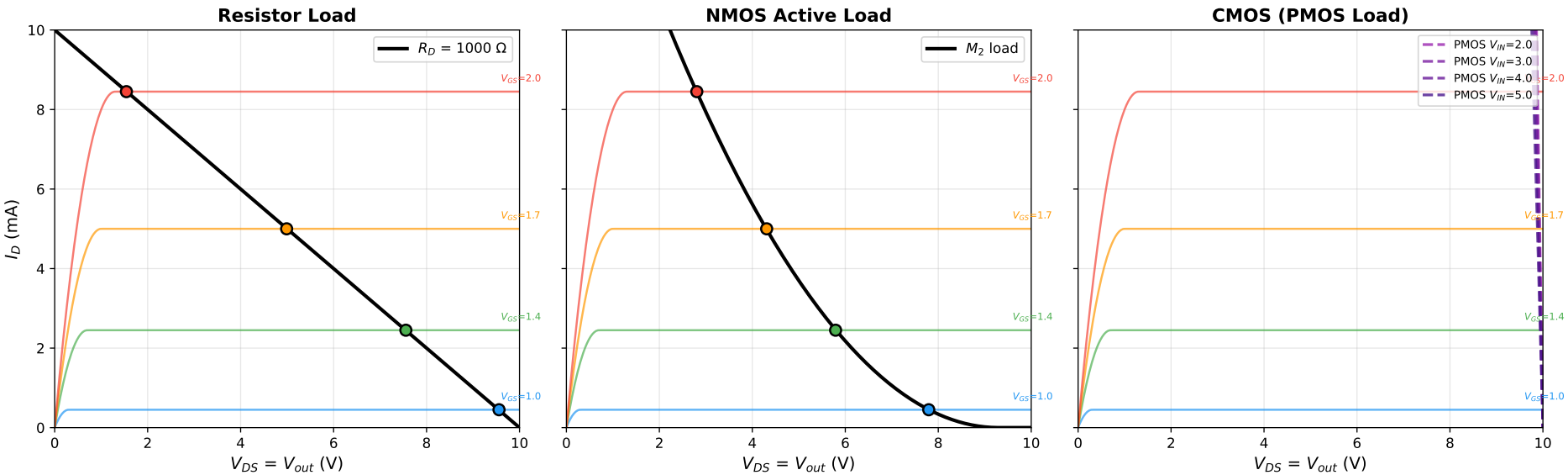
Gain Comparison

	Resistor ($R_D = 1\ \text{k}\Omega$)	**NMOS Active** ($W/L_2 = 4$)	**CMOS** (matched)
Gain formula	$-g_m R_D$	$-\sqrt{\frac{K_{n1}}{K_{n2}}}$	$-\infty$ ($\lambda = 0$)
$\lvert A_v \rvert$ **at** $V_{IN} = 1.7\mathbf{V}$	10	5	∞
Output swing	0 to V_{DD}	0 to $V_{DD} - V_{TN}$	0 to V_{DD}
Static power	$I_D \cdot V_{DD}$	$I_D \cdot V_{DD}$	≈ 0 at rails

CMOS wins on gain, output swing, **and** static power.

This is why CMOS dominates modern digital and analog IC design.

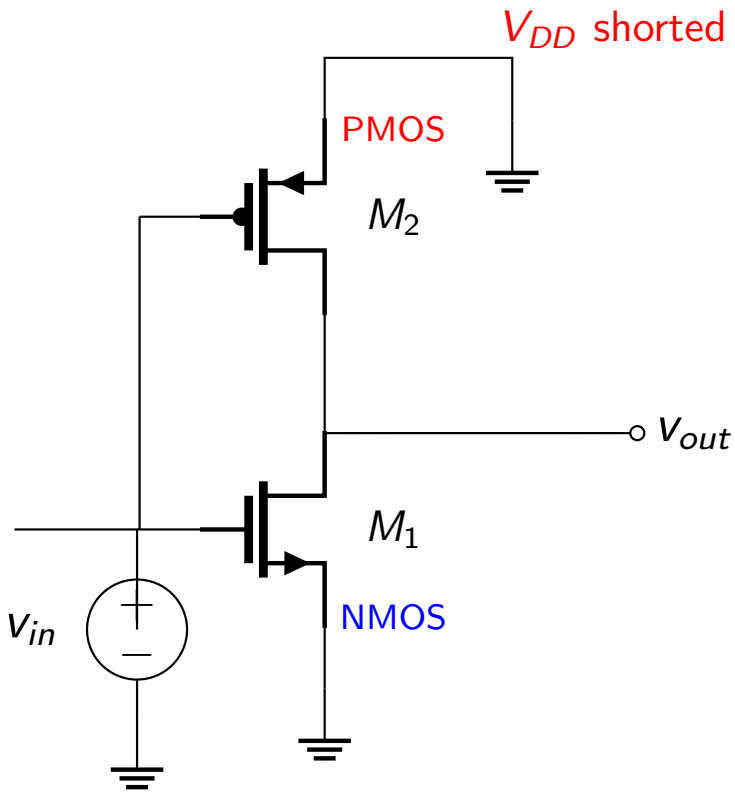
Load Line Comparison



CMOS Small-Signal Analysis

NMOS vs PMOS Small-Signal Models

Step 1: Short DC Sources



Short V_{DD} to ground. Both M_1's source **and** M_2's source are at AC ground.

$\Rightarrow$ For both transistors: $v_{gs} = v_{in} - 0 = v_{in}$

NMOS vs PMOS: Small-Signal Conventions

	NMOS (M_1)	**PMOS (M_2)**
Control voltage	$v_{gs} = V_G - V_S$	$v_{sg} = V_S - V_G$
Current source	$g_{mn}\, v_{gs}$, D $\rightarrow$ S	$g_{mp}\, v_{sg}$, S $\rightarrow$ D
g_m	$K_n(V_{GS} - V_{TN})$	$K_p(V_{SG} - \lvert V_{TP}\rvert)$
r_o	$1/(\lambda_n I_D)$	$1/(\lambda_p I_D)$

NMOS: $g_m v_{gs}$ flows **D** $\rightarrow$ **S** (same direction as DC current)
PMOS: $g_m v_{sg}$ flows **S** $\rightarrow$ **D** (same direction as DC current)

Both models use the convention where positive g_m times a positive control voltage produces current in the **same direction as DC**.

NMOS vs PMOS: Current Direction in CMOS

NMOS (M_1): $v_{gs1} = v_{in}$ (source at GND)

$g_{mn}\, v_{in}$ flows D $\rightarrow$ S = out of v_{out} to ground.
When $v_{in}\uparrow$: **more** current pulled out of v_{out}.

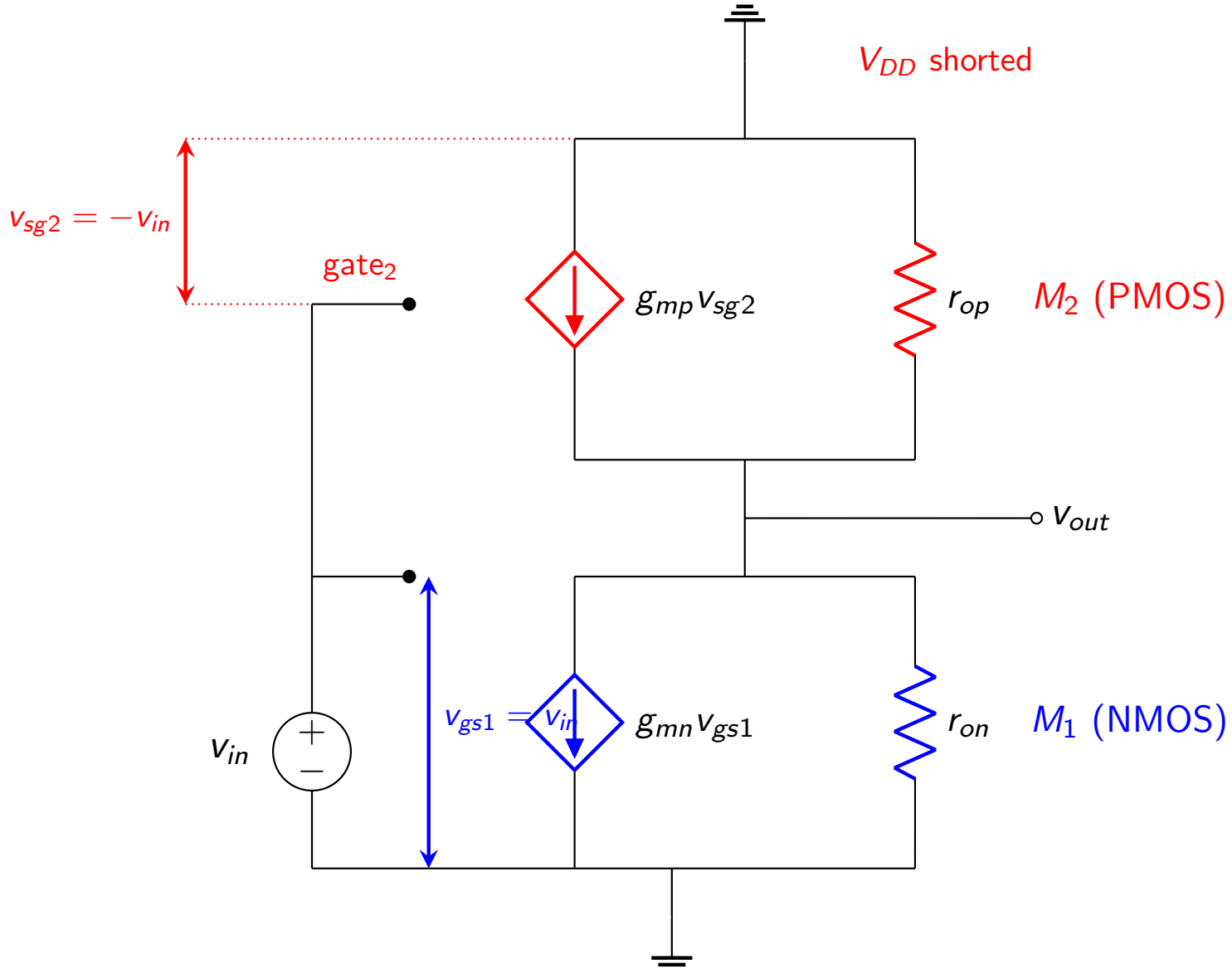
PMOS (M_2): $v_{sg2} = V_S - V_G = 0 - v_{in} = -v_{in}$ (source at AC gnd)

$g_{mp}\, v_{sg2} = g_{mp}(-v_{in})$ flows S $\rightarrow$ D = into v_{out}.
Negative $\Rightarrow$ current actually flows D $\rightarrow$ S = out of v_{out}!
When $v_{in}\uparrow$: **less** current supplied into v_{out}.

Both effects pull v_{out} down when v_{in} goes up:

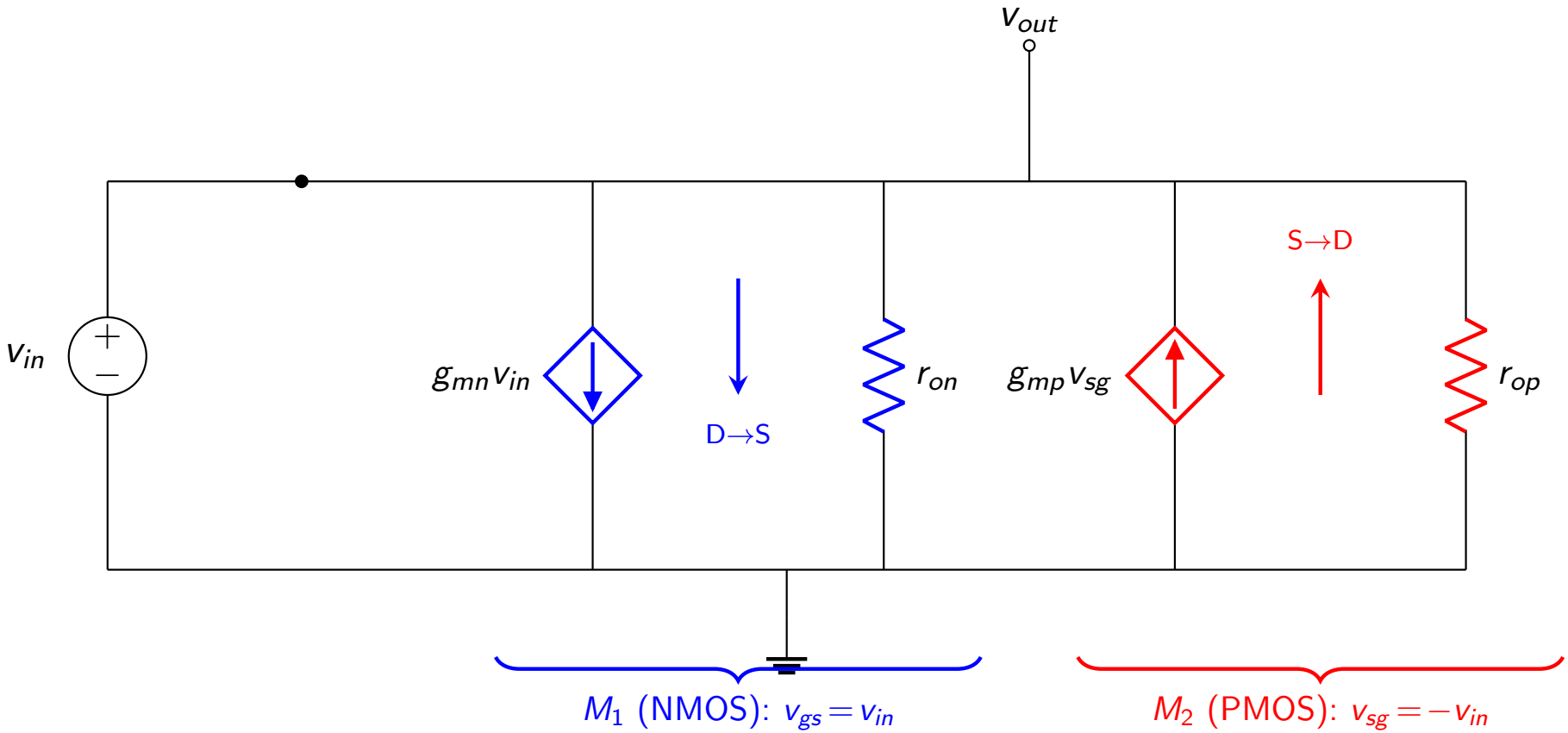
M_1 pulls **more** current out **AND** M_2 supplies **less** current in.

Step 2: Replace Each Transistor with Its Model



Key difference from NMOS active load: M_2's gate connects to v_{in}, **not**

Step 3: Simplified Equivalent Circuit



- NMOS: $g_{mn}v_{in}$ arrow **down** (D→S) PMOS: $g_{mp}v_{sg}$ arrow **up** (S→D)
- With $v_{sg} = -v_{in}$: both current sources pull current **out of** v_{out}
- All four elements in **parallel** between v_{out} and ground

Step 4: Voltage Gain Derivation

KCL at v_{out}. Current leaving through each element:

$$\underbrace{g_{mn}\, v_{in}}_{\text{NMOS } g_m} + \frac{v_{out}}{r_{on}} \underbrace{- g_{mp}\, v_{sg}}_{\text{PMOS } g_m} + \frac{v_{out}}{r_{op}} = 0$$

Substitute $v_{sg} = -v_{in}$:

$$g_{mn}\, v_{in} + \frac{v_{out}}{r_{on}} + g_{mp}\, v_{in} + \frac{v_{out}}{r_{op}} = 0$$

Both g_m terms have the **same sign** — they add!

$$\boxed{A_v = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp})(r_{on} \parallel r_{op})}$$

With $\lambda = 0$: $r_{on}, r_{op} \to \infty \;\Rightarrow\; |A_v| \to \infty$ ✓

Why CMOS Gain $\gg$ NMOS Active Load Gain

NMOS active load (diode-connected M_2):

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \parallel r_{o1}\right) \approx -\frac{g_{m1}}{g_{m2}}$$

M_2's g_{m2} appears in the **denominator** — it **limits** gain.

CMOS inverter (complementary M_2):

$$A_v = -(g_{mn} + g_{mp})(r_{on} \parallel r_{op})$$

M_2's g_{mp} appears in the **numerator** — it **boosts** gain!

Diode-connected load: M_2's gate is tied to its drain (v_{out}).
It senses the *output* $\Rightarrow$ negative feedback $\Rightarrow$ reduces gain.

CMOS load: M_2's gate is tied to the *input* (v_{in}).
It senses the *input* $\Rightarrow$ both transistors amplify $\Rightarrow$ gain adds!

Numerical Example ($\lambda \neq 0$)

Suppose $\lambda_n = \lambda_p = 0.02\ \text{V}^{-1}$ at $V_{IN} = V_M = 5$ V:

$I_D = \frac{K_n}{2}(V_M - V_{TN})^2 = \frac{10\times10^{-3}}{2}(4.3)^2 = 92.5$ mA

$g_{mn} = g_{mp} = K_n(V_M - V_{TN}) = 10 \times 10^{-3} \times 4.3 = 43$ mA/V

$r_{on} = r_{op} = \frac{1}{\lambda I_D} = \frac{1}{0.02\times0.0925} = 541\ \Omega$

	NMOS Active	**CMOS**
$\lvert A_v \rvert$	$g_{m1}/g_{m2} = 5$	$(g_{mn}+g_{mp})(r_{on}\|\|r_{op})$
		$= (86\ \text{mA/V})(270\ \Omega)$
	5	**23.2**

CMOS gain is nearly 5× higher — and this gap grows with smaller λ.

Summary: Three Load Strategies

Resistor Load (R_D)

$$V_{out} = V_{DD} - \frac{K_n R_D}{2}(V_{IN} - V_{TN})^2 \qquad A_v = -g_m R_D$$

NMOS Active Load (diode-connected M_2)

$$V_{out} = V_{DD} - V_{TN} - \sqrt{\frac{K_{n1}}{K_{n2}}}(V_{IN} - V_{TN}) \qquad A_v = -\sqrt{\frac{K_{n1}}{K_{n2}}}$$

CMOS Inverter (complementary PMOS load)

$$V_M = \frac{V_{TN} + \sqrt{K_p/K_n}\,(V_{DD} - |V_{TP}|)}{1 + \sqrt{K_p/K_n}} \qquad A_v \to -\infty \ (\lambda = 0)$$

The more the load responds to V_{IN}, the higher the gain.

R_D: no response $\longrightarrow$ Diode NMOS: no response $\longrightarrow$ PMOS: full response