EE461g: Introduction to Electronic Circuits

Lecture 16

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Outline

MOSFET Voltage Dividers

Setting voltages with transistor sizing

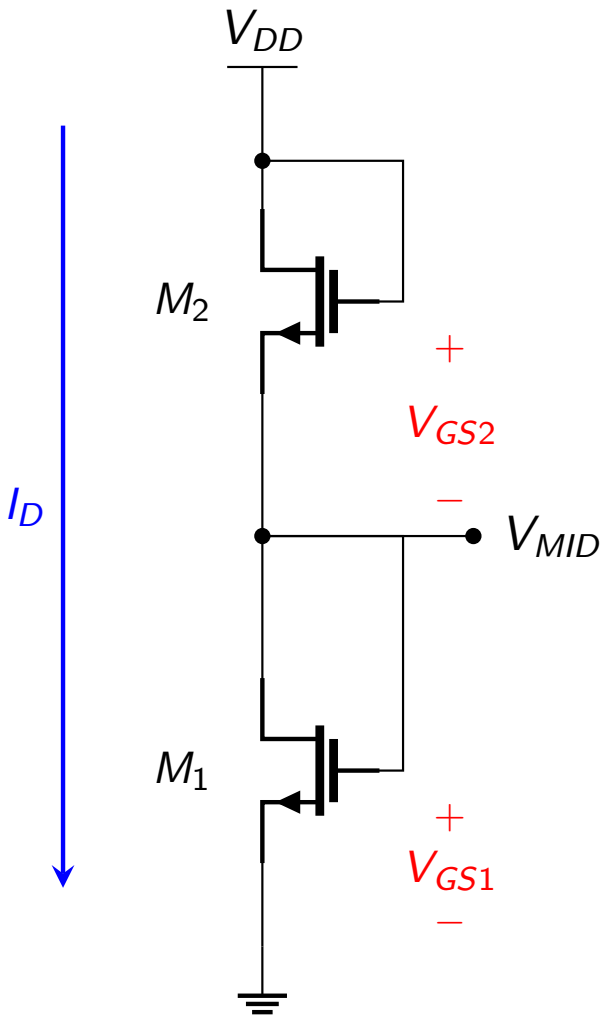
Motivation: Why a MOSFET Voltage Divider?

- Resistor voltage dividers require **large silicon area**
- MOSFETs can act as voltage-setting elements with **much smaller area**
- The output voltage is controlled by the **W/L ratios** of the transistors
- This is the foundation for:
  - Bias generation in analog circuits
  - Reference voltage circuits
  - Understanding CMOS inverter switching threshold

Key idea: Two diode-connected MOSFETs in series act like a voltage divider, but the "ratio" is set by transistor sizes, not resistance values.

NMOS–NMOS Voltage Divider

Two Diode-Connected NMOS in Series



Both MOSFETs are wired as **active loads** with the gate tied to the drain ($V_{GS} = V_{DS}$). Current flows as long as the voltage across each device $> V_{TN}$, which guarantees **saturation**. Same I_D flows through both.

Voltages:

- M_1: $V_{GS1} = V_{MID}$
- M_2: $V_{GS2} = V_{DD} - V_{MID}$

Parameters:

- M_1: $K_{n1} = k'_n \cdot (W/L)_1$
- M_2: $K_{n2} = k'_n \cdot (W/L)_2$
- Same V_{TN} for both

NMOS–NMOS Divider: Derivation

Both in saturation ($\lambda = 0$):

$$I_{D1} = \frac{K_{n1}}{2}(V_{GS1} - V_{TN})^2 \qquad I_{D2} = \frac{K_{n2}}{2}(V_{GS2} - V_{TN})^2$$

KCL: $I_{D1} = I_{D2}$ (series circuit, same current)

$$\frac{K_{n1}}{2}(V_{MID} - V_{TN})^2 = \frac{K_{n2}}{2}(V_{DD} - V_{MID} - V_{TN})^2$$

Take the square root (both sides positive):

$$\sqrt{K_{n1}}\,(V_{MID} - V_{TN}) = \sqrt{K_{n2}}\,(V_{DD} - V_{MID} - V_{TN})$$

The $\frac{1}{2}$ cancels. The square root turns the quadratic into a **linear** equation in V_{MID}!

NMOS–NMOS Divider: Solving for V_{MID}

Define the **sizing ratio**:

$$\boxed{R = \sqrt{\frac{K_{n2}}{K_{n1}}} = \sqrt{\frac{(W/L)_2}{(W/L)_1}}}$$

Then:

$$\begin{aligned} V_{MID} - V_{TN} &= R\,(V_{DD} - V_{MID} - V_{TN}) \\ V_{MID} - V_{TN} &= R \cdot V_{DD} - R \cdot V_{MID} - R \cdot V_{TN} \\ V_{MID}(1+R) &= R \cdot V_{DD} + V_{TN}(1-R) \end{aligned}$$

$$\boxed{V_{MID} = \frac{R \cdot V_{DD} + V_{TN}(1-R)}{1+R}}$$

NMOS–NMOS Divider: Special Cases

$$V_{MID} = \frac{R \cdot V_{DD} + V_{TN}(1 - R)}{1 + R} \qquad \text{where } R = \sqrt{\frac{(W/L)_2}{(W/L)_1}}$$

Condition	R	V_{MID}
$(W/L)_1 = (W/L)_2$	$R = 1$	$\frac{V_{DD}}{2}$
$(W/L)_1 \gg (W/L)_2$	$R \to 0$	$\to V_{TN}$
$(W/L)_1 \ll (W/L)_2$	$R \to \infty$	$\to V_{DD} - V_{TN}$

Intuition: A wider transistor has lower V_{GS} for the same current.
Making M_1 wider $\Rightarrow$ smaller $V_{GS1} \Rightarrow V_{MID}$ drops toward V_{TN}.
Making M_2 wider $\Rightarrow$ smaller $V_{GS2} \Rightarrow V_{MID}$ rises toward $V_{DD} - V_{TN}$.

Power Dissipation: We Want Less!

Both dividers draw current from V_{DD}, dissipating $P = V_{DD} \cdot I$.

Resistor Divider

$$\boxed{P = \frac{V_{DD}^2}{R_1 + R_2}}$$

To reduce power $\Rightarrow$ increase $R_1 + R_2$
$\Rightarrow$ **larger resistors** $\Rightarrow$ **more area**

NMOS Divider

$$\boxed{P = V_{DD} \cdot \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{MID} - V_{TN})^2}$$

Reduce power $\Rightarrow$ decrease $(W/L)_1$
$\Rightarrow$ **smaller transistors, less area**

MOSFET advantage: Scaling both $(W/L)_1$ and $(W/L)_2$ down by the same factor keeps V_{MID} constant but **reduces power and area**.

With resistors, reducing power means *increasing* area!

NMOS–NMOS Divider: Numerical Example

Given: $V_{DD} = 5$ V, $V_{TN} = 0.7$ V, $k_n' = 200\ \mu$A/V^2

Design goal: Set $V_{MID} = 2.5$ V

Solution: Choose $R = 1 \Rightarrow (W/L)_1 = (W/L)_2$

$$V_{MID} = \frac{1 \cdot 5 + 0.7(1-1)}{1+1} = \frac{5}{2} = 2.5 \text{ V} \quad \checkmark$$

Design goal: Set $V_{MID} = 1.5$ V

Solution: Solve for R:

$$1.5 = \frac{5R + 0.7(1-R)}{1+R} \Rightarrow 1.5(1+R) = 5R + 0.7 - 0.7R$$

$$1.5 + 1.5R = 4.3R + 0.7 \Rightarrow 0.8 = 2.8R \Rightarrow R = 0.286$$

$$\frac{(W/L)_2}{(W/L)_1} = R^2 = 0.0816 \Rightarrow \text{e.g., } (W/L)_1 = 100,\ (W/L)_2 = 8.16$$

NMOS–NMOS Divider: What About the Current?

Once V_{MID} is known, the current is:

$$\boxed{I_D = \frac{K_{n1}}{2}(V_{MID} - V_{TN})^2 = \frac{k'_n}{2} \cdot \left(\frac{W}{L}\right)_1 (V_{MID} - V_{TN})^2}$$

From the previous example ($V_{MID} = 1.5$ V):

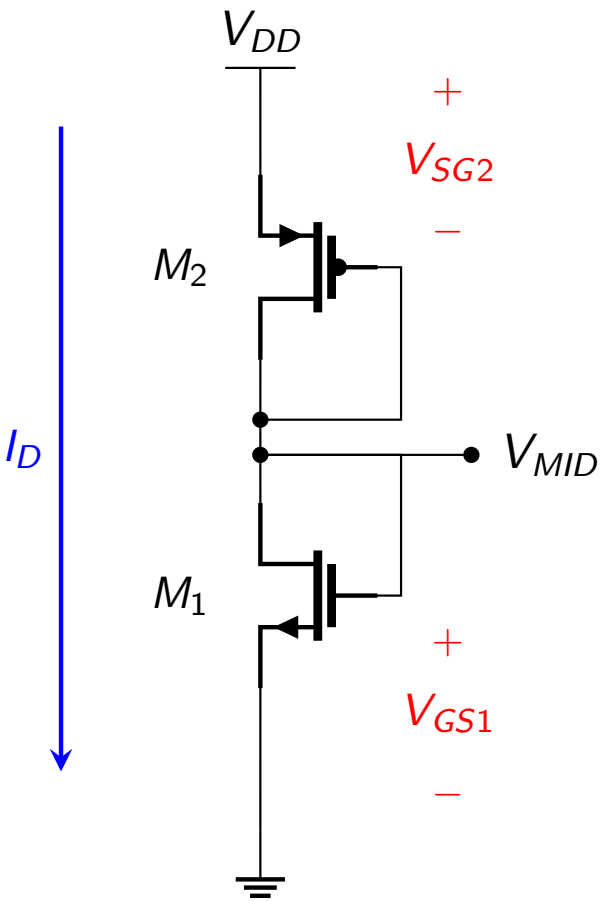
$$I_D = \frac{200 \times 10^{-6}}{2} \cdot 100 \cdot (1.5 - 0.7)^2 = 10 \text{ mA} \cdot 0.64 = 6.4 \text{ mA}$$

Important: The W/L ratio sets V_{MID}, but the **absolute** W/L values set the current.

Scaling both $(W/L)_1$ and $(W/L)_2$ by the same factor keeps V_{MID} the same but changes I_D.

PMOS–NMOS Voltage Divider

Diode-Connected PMOS on Top, NMOS on Bottom



Now replace the top NMOS with a **PMOS** active load (gate tied to drain). Current flows as long as $V_{SG2} > |V_{TP}|$.

Voltages:

- M_1 (NMOS): $V_{GS1} = V_{MID}$
- M_2 (PMOS): $V_{SG2} = V_{DD} - V_{MID}$

Parameters:

- M_1: $K_{n1} = k'_n \cdot (W/L)_1$, threshold V_{TN}
- M_2: $K_{p2} = k'_p \cdot (W/L)_2$, threshold $|V_{TP}|$

This is the **CMOS** topology!

PMOS–NMOS Divider: Derivation

Saturation currents ($\lambda = 0$):

M_1 (NMOS):

$$I_{D1} = \frac{K_{n1}}{2}(V_{GS1} - V_{TN})^2 = \frac{K_{n1}}{2}(V_{MID} - V_{TN})^2$$

M_2 (PMOS):

$$I_{D2} = \frac{K_{p2}}{2}(V_{SG2} - |V_{TP}|)^2 = \frac{K_{p2}}{2}(V_{DD} - V_{MID} - |V_{TP}|)^2$$

KCL: $I_{D1} = I_{D2}$

$$\frac{K_{n1}}{2}(V_{MID} - V_{TN})^2 = \frac{K_{p2}}{2}(V_{DD} - V_{MID} - |V_{TP}|)^2$$

Taking the square root:

$$\sqrt{K_{n1}}\,(V_{MID} - V_{TN}) = \sqrt{K_{p2}}\,(V_{DD} - V_{MID} - |V_{TP}|)$$

PMOS–NMOS Divider: Solving for V_{MID}

Define the **sizing ratio**:

$$\boxed{R = \sqrt{\frac{K_{p2}}{K_{n1}}} = \sqrt{\frac{k'_p \cdot (W/L)_2}{k'_n \cdot (W/L)_1}}}$$

Then:

$$V_{MID} - V_{TN} = R\,(V_{DD} - V_{MID} - |V_{TP}|)$$
$$V_{MID}(1 + R) = V_{TN} + R\,(V_{DD} - |V_{TP}|)$$

$$\boxed{V_{MID} = \frac{R\,(V_{DD} - |V_{TP}|) + V_{TN}}{1 + R}}$$

Note: R now involves **both** k'_n and k'_p since the transistors are different types.

PMOS–NMOS Divider: Special Cases

$$V_{MID} = \frac{R\,(V_{DD} - |V_{TP}|) + V_{TN}}{1 + R} \qquad \text{where } R = \sqrt{\frac{K_{p2}}{K_{n1}}}$$

Condition	R	V_{MID}
$K_{n1} = K_{p2}$	$R = 1$	$\frac{V_{DD} - \|V_{TP}\| + V_{TN}}{2}$
$K_{n1} \gg K_{p2}$	$R \to 0$	$\to V_{TN}$
$K_{n1} \ll K_{p2}$	$R \to \infty$	$\to V_{DD} - \|V_{TP}\|$

If $V_{TN} = |V_{TP}|$ and $K_{n1} = K_{p2}$:

$V_{MID} = V_{DD}/2$ (symmetric CMOS!)

Comparison: NMOS–NMOS vs PMOS–NMOS

	NMOS–NMOS	**PMOS–NMOS**
V_{MID}	$\frac{R \cdot V_{DD} + V_{TN}(1-R)}{1+R}$	$\frac{R(V_{DD} - \lvert V_{TP}\rvert) + V_{TN}}{1+R}$
R defined as	$\sqrt{K_{n2}/K_{n1}}$	$\sqrt{K_{p2}/K_{n1}}$
Range	V_{TN} to $V_{DD} - V_{TN}$	V_{TN} to $V_{DD} - \lvert V_{TP}\rvert$
$R = 1$ result	$V_{DD}/2$	$\frac{V_{DD} - \lvert V_{TP}\rvert + V_{TN}}{2}$
Process params	k'_n only	k'_n and k'_p

In both cases: V_{MID} is set by the **ratio** of transistor sizes, and the **absolute** sizes set the current.

PMOS–NMOS Divider: Numerical Example

Given: $V_{DD} = 5$ V, $V_{TN} = 0.7$ V, $|V_{TP}| = 0.8$ V, $k'_n = 200\ \mu\text{A/V}^2$, $k'_p = 80\ \mu\text{A/V}^2$

Design goal: $V_{MID} = V_{DD}/2 = 2.5$ V. Solve for R:

$$2.5 = \frac{4.2R + 0.7}{1 + R} \Rightarrow 2.5 + 2.5R = 4.2R + 0.7 \Rightarrow R = 1.059$$

$$R^2 = \frac{K_{p2}}{K_{n1}} = \frac{k'_p(W/L)_2}{k'_n(W/L)_1} = 1.121 \Rightarrow \frac{(W/L)_2}{(W/L)_1} = 1.121 \cdot \frac{200}{80} = 2.80$$

The PMOS must be 2.8× wider than the NMOS to get $V_{MID} = V_{DD}/2$
(because $k'_p < k'_n$, the PMOS is inherently weaker)

NMOS Current Mirror

Copying current with matched transistors

From Voltage Divider to Current Mirror

What we have:

The diode-connected M_1 in our voltage divider sets a specific V_{GS1}:

$$V_{GS1} = V_{MID}$$

which produces a current:

$$I_{REF} = \frac{K_{n1}}{2}(V_{GS1} - V_{TN})^2$$

Key idea:

If we connect a **second NMOS** (M_3) with its gate tied to the same node, it sees the **same** V_{GS}:

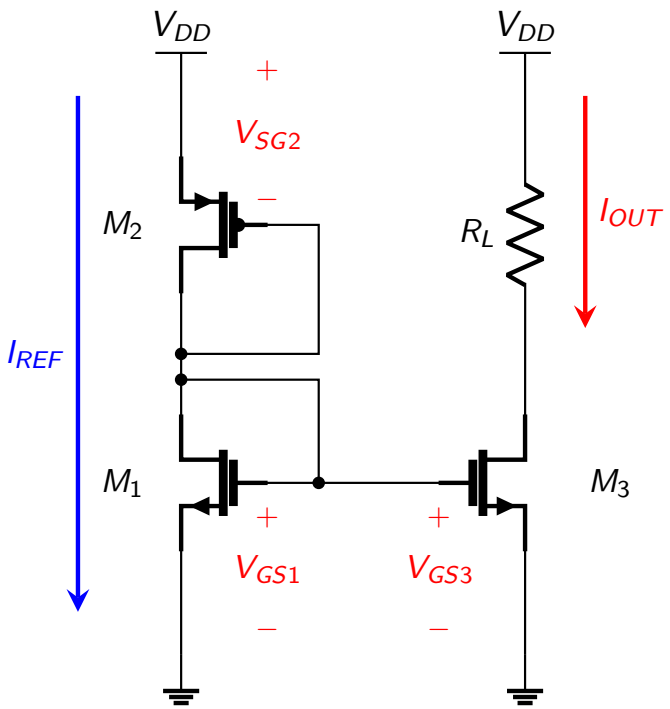
$$V_{GS3} = V_{GS1} = V_{MID}$$

So M_3 carries:

$$I_{OUT} = \frac{K_{n3}}{2}(V_{GS3} - V_{TN})^2$$

Same V_{GS}, same equation $\Rightarrow$ the current ratio depends only on $K_{n3}/K_{n1} = (W/L)_3/(W/L)_1$

NMOS Current Mirror Circuit



M_2 (PMOS) and M_1 (NMOS) form the divider (diode-connected). M_3 shares V_{GS} with M_1.

Both M_1 and M_3 in saturation ($\lambda = 0$):

$$I_{REF} = \frac{K_{n1}}{2}(V_{GS} - V_{TN})^2, \quad I_{OUT} = \frac{K_{n3}}{2}(V_{GS} -$$

Current ratio:

$$\boxed{\frac{I_{OUT}}{I_{REF}} = \frac{K_{n3}}{K_{n1}} = \frac{(W/L)_3}{(W/L)_1}}$$

If $(W/L)_3 = (W/L)_1$: $I_{OUT} = I_{REF}$
The current is **mirrored**!

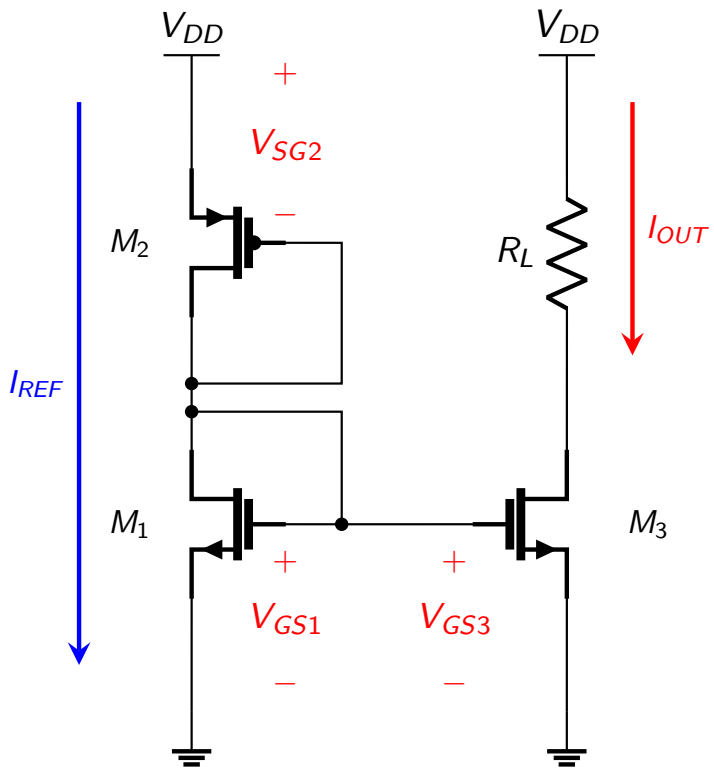
Current Mirror: Scaling the Current

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_3}{(W/L)_1}$$

$(W/L)_3$ **vs** $(W/L)_1$	**Ratio**	**Result**
$(W/L)_3 = (W/L)_1$	1:1	$I_{OUT} = I_{REF}$ (copy)
$(W/L)_3 = 2\,(W/L)_1$	2:1	$I_{OUT} = 2\,I_{REF}$ (amplify)
$(W/L)_3 = \frac{1}{2}(W/L)_1$	1:2	$I_{OUT} = \frac{1}{2}\,I_{REF}$ (reduce)

A single reference current I_{REF} can generate **multiple different currents** by using mirror transistors with different W/L ratios.

Putting It Together: Divider + Mirror



The voltage divider (M_2, M_1) sets V_{MID} and I_{REF}.

The mirror transistor M_3 copies (or scales) that current:

$$I_{OUT} = I_{REF} \cdot \frac{(W/L)_3}{(W/L)_1}$$

Design procedure:

1. Choose $(W/L)_1$, $(W/L)_2$ ratio to set V_{MID}
2. Choose absolute sizes to set I_{REF}
3. Choose $(W/L)_3$ to set I_{OUT}

Current Mirror: When Does It Work?

For M_3 to mirror accurately, it must be in **saturation**:

$$V_{DS3} \geq V_{GS} - V_{TN} = V_{MID} - V_{TN}$$

- M_1 is **always** in saturation (diode-connected: $V_{DS1} = V_{GS1}$)
- M_3 saturation depends on the circuit connected to its drain
- If V_{OUT} drops below $V_{MID} - V_{TN}$, M_3 enters **triode** and I_{OUT} decreases

Compliance range: The mirror output is accurate for
$V_{OUT} \geq V_{GS} - V_{TN} = V_{OV}$ (the overdrive voltage)

With $\lambda \neq 0$: I_{OUT} varies slightly with V_{DS3} due to channel-length modulation.
Output resistance of the mirror: $r_{o3} = 1/(\lambda I_{OUT})$

Maximum Load Resistor R_L

With R_L connected from V_{DD} to the drain of M_3:

$$V_{DS3} = V_{DD} - I_{OUT} \cdot R_L$$

For M_3 to remain in saturation:

$$V_{DS3} \geq V_{GS3} - V_{TN} = V_{MID} - V_{TN} = V_{OV}$$

Substituting:

$$V_{DD} - I_{OUT} \cdot R_L \geq V_{OV}$$

Solving for R_L:

$$\boxed{R_{L,\text{max}} = \frac{V_{DD} - V_{OV}}{I_{OUT}} = \frac{V_{DD} - (V_{MID} - V_{TN})}{I_{OUT}}}$$

Larger $R_L \Rightarrow$ more voltage drop $\Rightarrow$ lower $V_{DS3} \Rightarrow M_3$ pushed toward triode

What If R_L Changes?

Suppose R_L varies by $\pm 10\%$ due to temperature or manufacturing tolerance.

With an **ideal** current source ($\lambda = 0$):

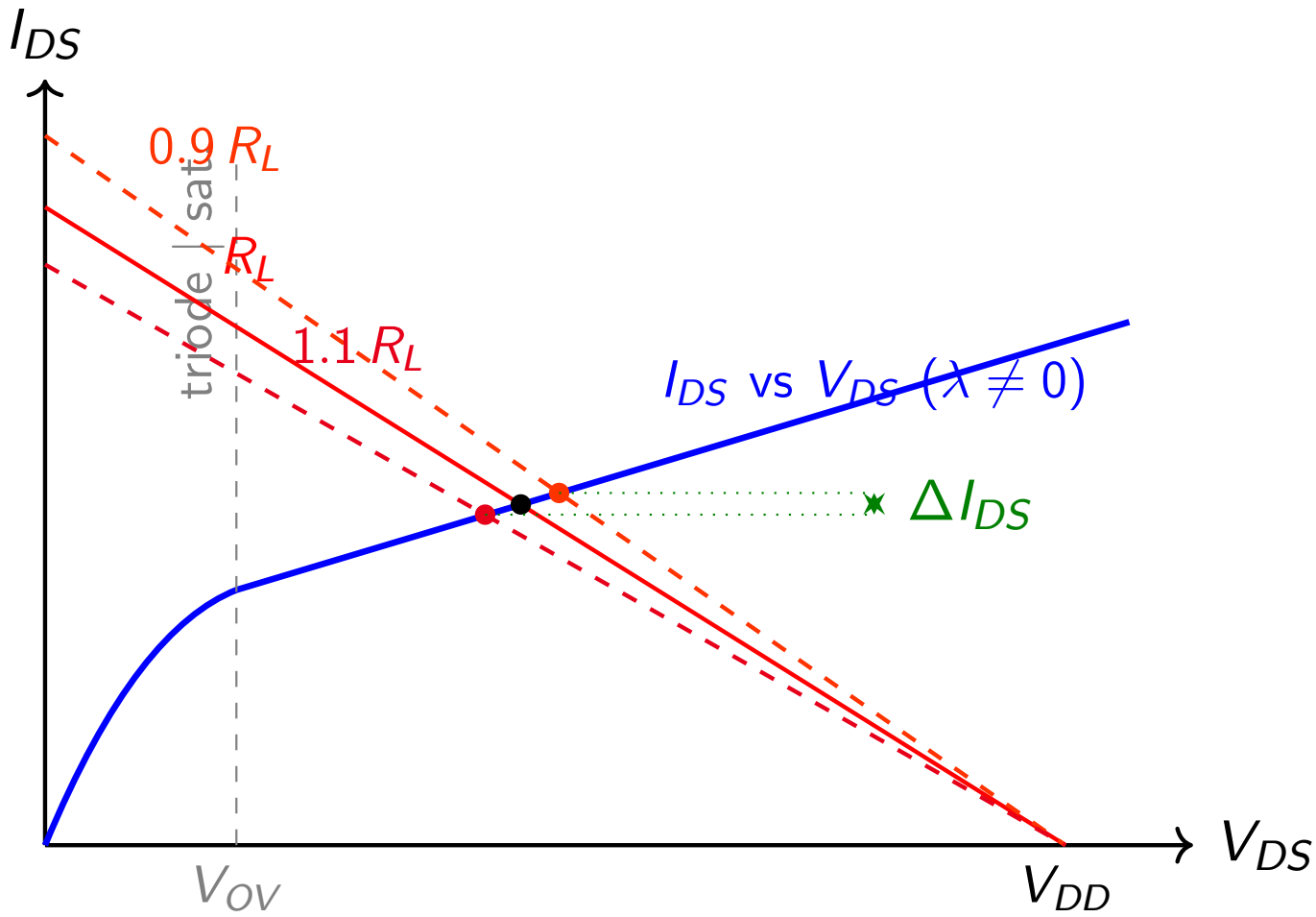
- I_{OUT} depends only on V_{GS} and $(W/L)_3$ — not on V_{DS3}
- Changing R_L changes V_{DS3} but **not** I_{OUT}
- The current is perfectly constant

With a **real** MOSFET ($\lambda \neq 0$):

$$I_{OUT} = \frac{K_{n3}}{2}(V_{GS} - V_{TN})^2 (1 + \lambda V_{DS3})$$

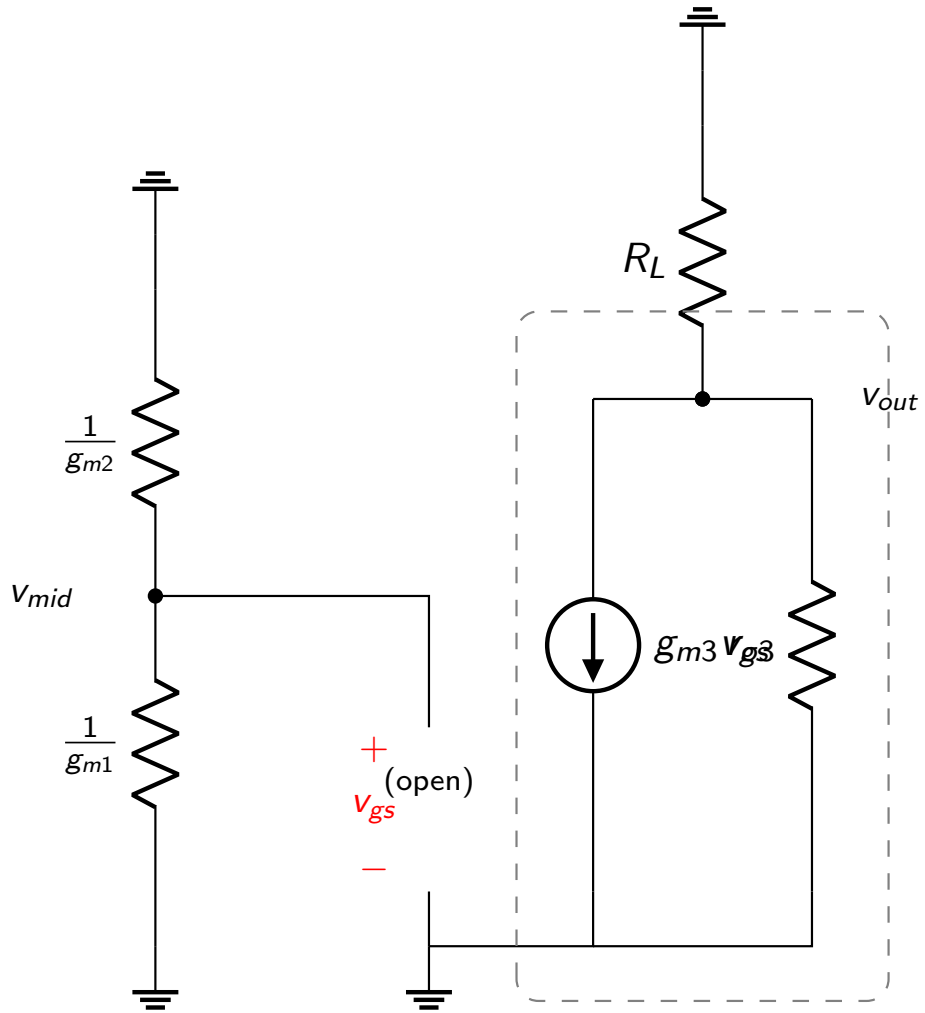
- $V_{DS3} = V_{DD} - I_{OUT} \cdot R_L$, so changing R_L changes V_{DS3}
- Changing V_{DS3} changes I_{OUT} through the λ term
- **How much** does I_{OUT} change? $\Rightarrow$ We need a **small-signal model**!

Graphical View: Load Line Meets MOSFET Curve



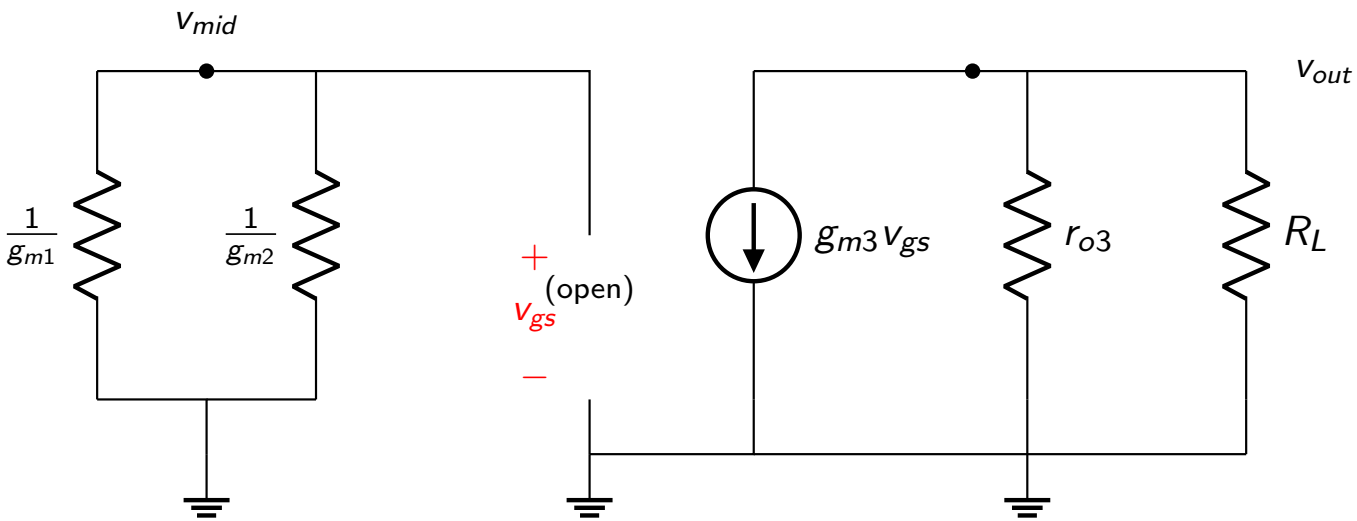
The slope in saturation $(1/r_o)$ means load line shifts cause ΔI_{DS}.
With $\lambda = 0$ the curve would be flat and $\Delta I_{DS} = 0$.

Small-Signal Model of the Current Mirror



Simplified Small-Signal Model

Since V_{DD} and GND are both AC ground, $\frac{1}{g_{m2}}$ folds down in parallel with $\frac{1}{g_{m1}}$, and $R_L \| r_{o3}$:



Simplifying: $v_{gs} = 0$

The gate of M_3 is connected to the divider output v_{mid}.

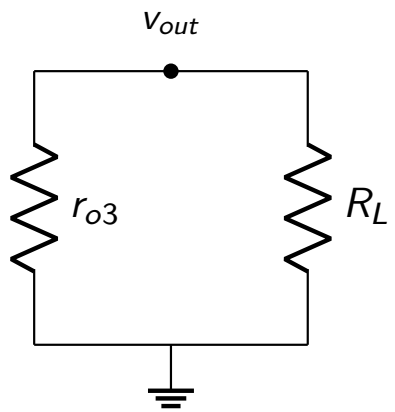
But v_{mid} is set by $\frac{1}{g_{m1}} \| \frac{1}{g_{m2}}$ connected between two AC grounds — so:

$$v_g = v_{mid} = 0 \quad \Rightarrow \quad v_{gs} = v_g - v_s = 0 - 0 = 0$$

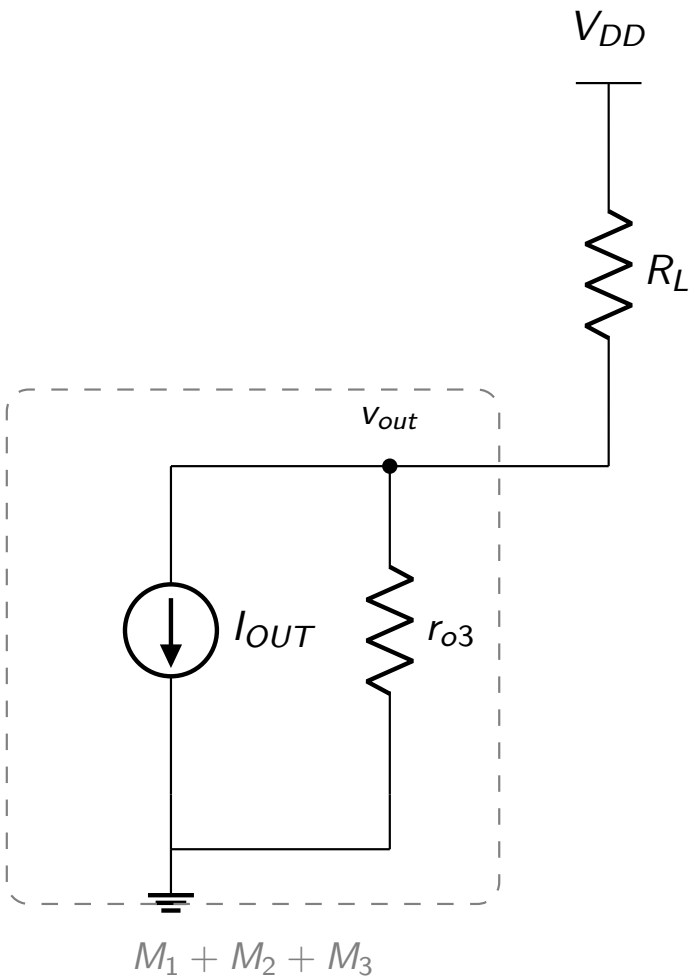
Since $v_{gs} = 0$:

$$g_{m3}\, v_{gs} = 0 \quad \Rightarrow \quad \text{current source becomes an } \textbf{open circuit}$$

The circuit reduces to just $r_{o3} \| R_L$:



Norton Equivalent of the Current Mirror



Replace all three MOSFETs with their Norton equivalent:

- **Current source:**
  $$I_{OUT} = I_{REF} \cdot \frac{(W/L)_3}{(W/L)_1}$$
- **Output resistance:**
  $$r_{o3} = \frac{1}{\lambda I_{OUT}}$$
- **Load:** R_L connects to V_{DD}

The current mirror looks like an **ideal current source** I_{OUT} in parallel with r_{o3}.

Intuition: What Is the Current Mirror Actually Doing?

The current source I_{OUT} is not *pulling* current down through R_L — it is **holding it back**.

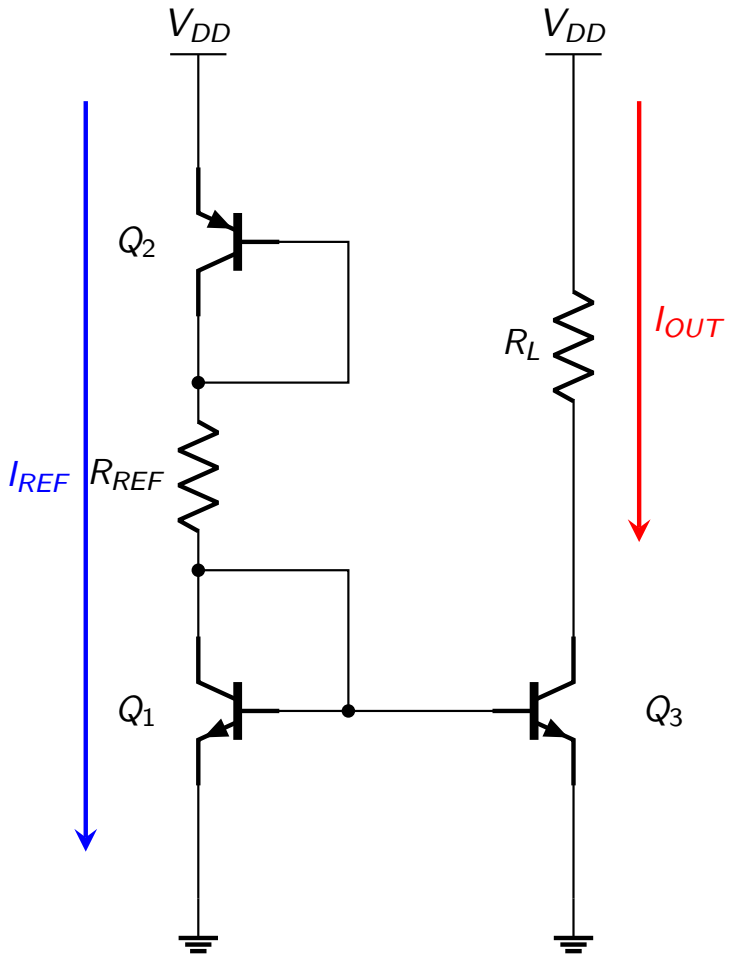
- Without the current mirror, R_L is connected between V_{DD} and ground, so the current would be:

$$I_{R_L} = \frac{V_{DD}}{R_L} > I_{OUT}$$

  The mirror **limits** the current to $I_{OUT} < \frac{V_{DD}}{R_L}$.
- What if $\frac{V_{DD}}{R_L} < I_{OUT}$? Since $I_{OUT} = I_{DS}$, the MOSFET cannot sustain that much current with the available voltage across R_L. The MOSFET leaves saturation and enters the **triode region** — the current mirror no longer works as designed.

The current mirror works only when R_L is small enough that $\frac{V_{DD}}{R_L} > I_{OUT}$, keeping M_3 in saturation.

BJT Version: PNP + Resistor + NPN with Current Mirror



BJT Reference Current: I_{REF}

Both Q_1 and Q_2 are diode-connected ($V_{CE} = V_{BE}$), so they are in the **active region**.

KVL around the left loop:

$$V_{DD} = V_{EB2} + I_{REF} \cdot R_{REF} + V_{BE1}$$

Solving for I_{REF}:

$$\boxed{I_{REF} = \frac{V_{DD} - V_{BE1} - V_{EB2}}{R_{REF}}}$$

With typical silicon BJTs ($V_{BE} \approx V_{EB} \approx 0.7\,\text{V}$):

$$I_{REF} \approx \frac{V_{DD} - 1.4\,\text{V}}{R_{REF}}$$

Unlike the MOSFET divider, I_{REF} is set by R_{REF} — not by transistor sizing!
The BJT V_{BE} is nearly fixed, so the resistor does all the work.

BJT Current Mirror: I_{OUT}

Q_1 and Q_3 share the same V_{BE}. The collector current of a BJT:

$$I_C = I_S\, e^{V_{BE}/V_T}$$

For Q_1 and Q_3:

$$I_{REF} \approx I_{S1}\, e^{V_{BE}/V_T}, \qquad I_{OUT} = I_{S3}\, e^{V_{BE}/V_T}$$

Taking the ratio:

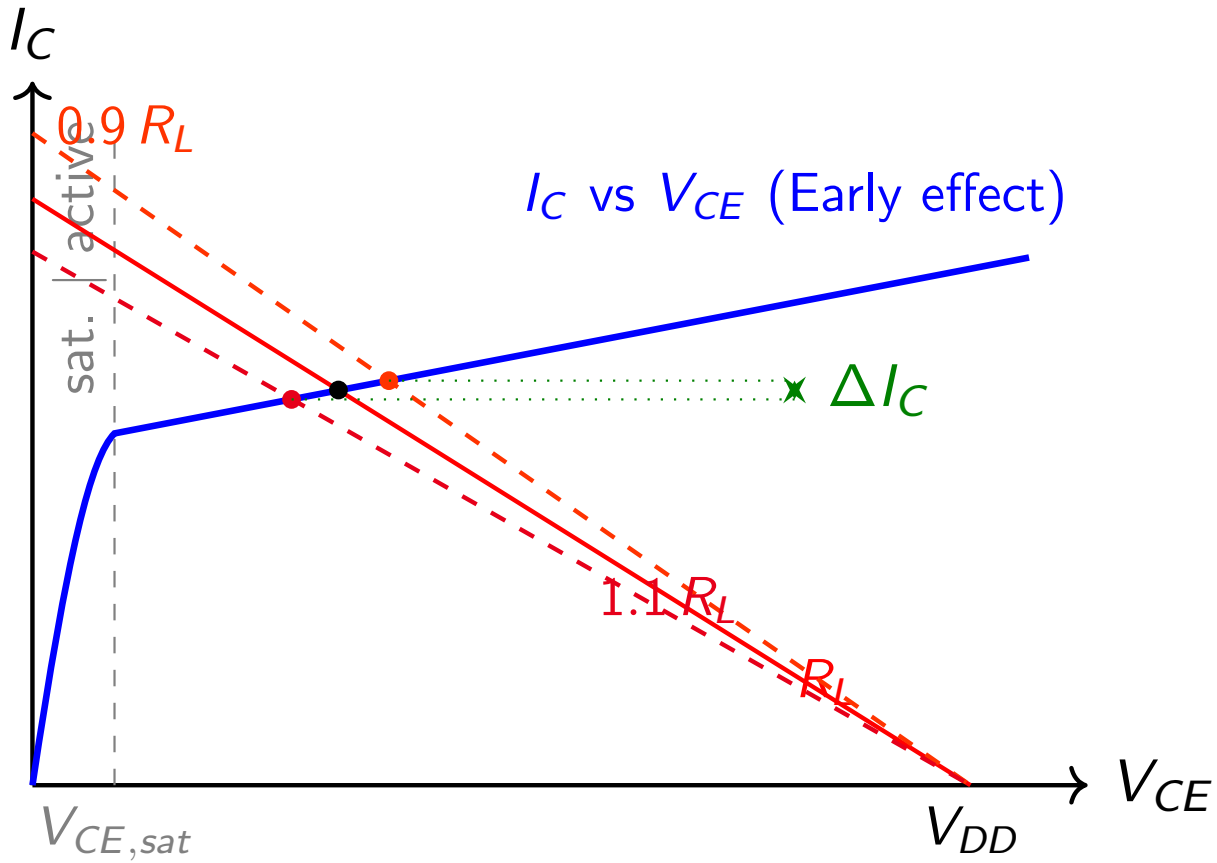
$$\boxed{\frac{I_{OUT}}{I_{REF}} = \frac{I_{S3}}{I_{S1}} = \frac{A_3}{A_1}}$$

where A is the emitter area of each transistor.
If Q_1 and Q_3 are **identical** ($A_3 = A_1$):

$$I_{OUT} = I_{REF} = \frac{V_{DD} - 1.4\,\text{V}}{R_{REF}}$$

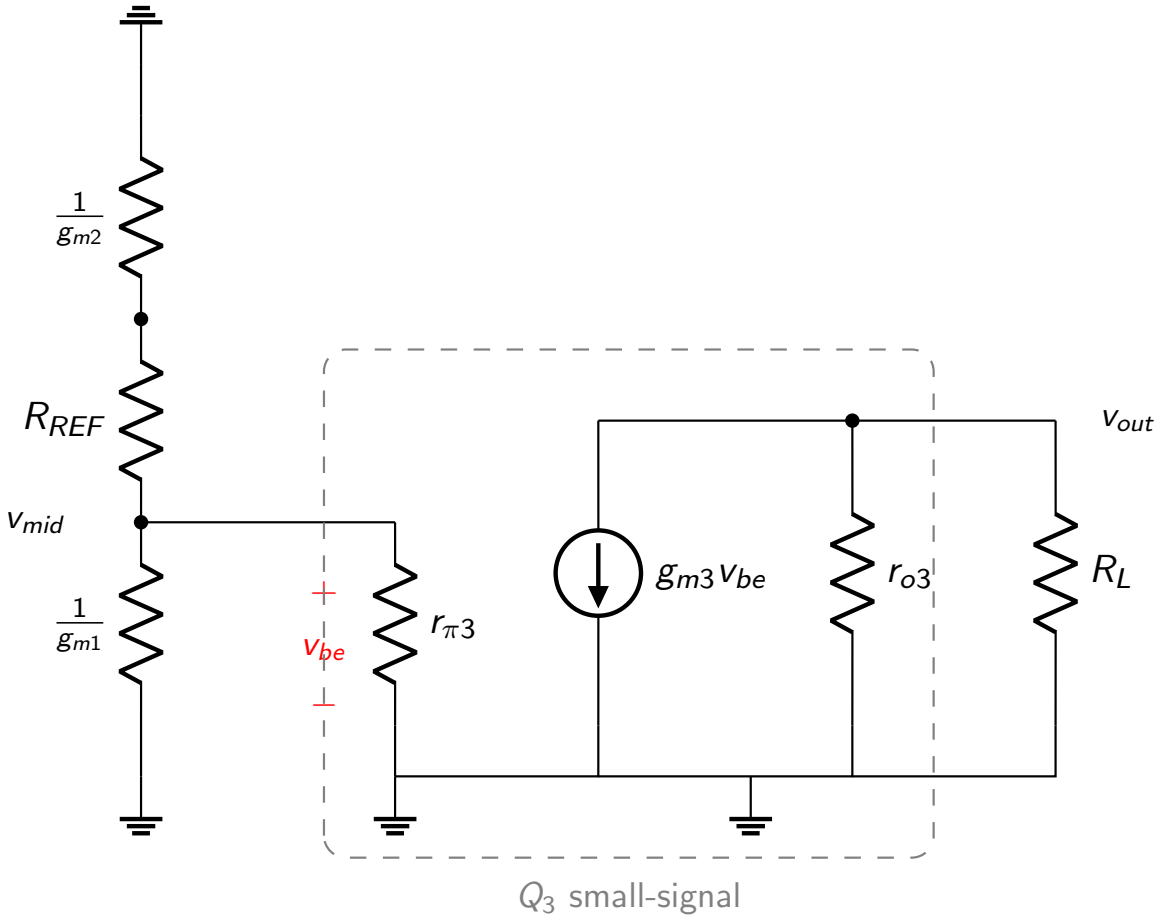
MOSFET mirror: scale current by W/L ratio (easy to adjust)
BJT mirror: scale current by emitter area ratio (harder to adjust)

BJT: Load Line Meets I_C vs V_{CE} Curve



The slope in the active region ($1/r_o = I_C/V_A$) is **steeper** than the MOSFET (λ is larger), so ΔI_C is larger for the same ΔR_L.

BJT Small-Signal Model of Q_3



Unlike the MOSFET, r_π draws base current $i_b = v_{be}/r_\pi$, which loads the bias network.
MOSFET gate draws **zero** current (open circuit).

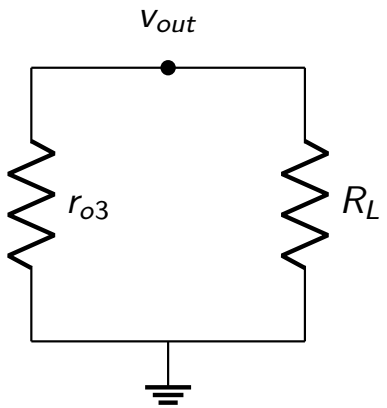
Simplifying: $v_{be} = 0$

v_{mid} is set by $\frac{1}{g_{m1}}$, R_{REF}, $\frac{1}{g_{m2}}$ between two AC grounds. Even though $r_{\pi 3}$ loads the node, v_{mid} is still driven to AC ground:

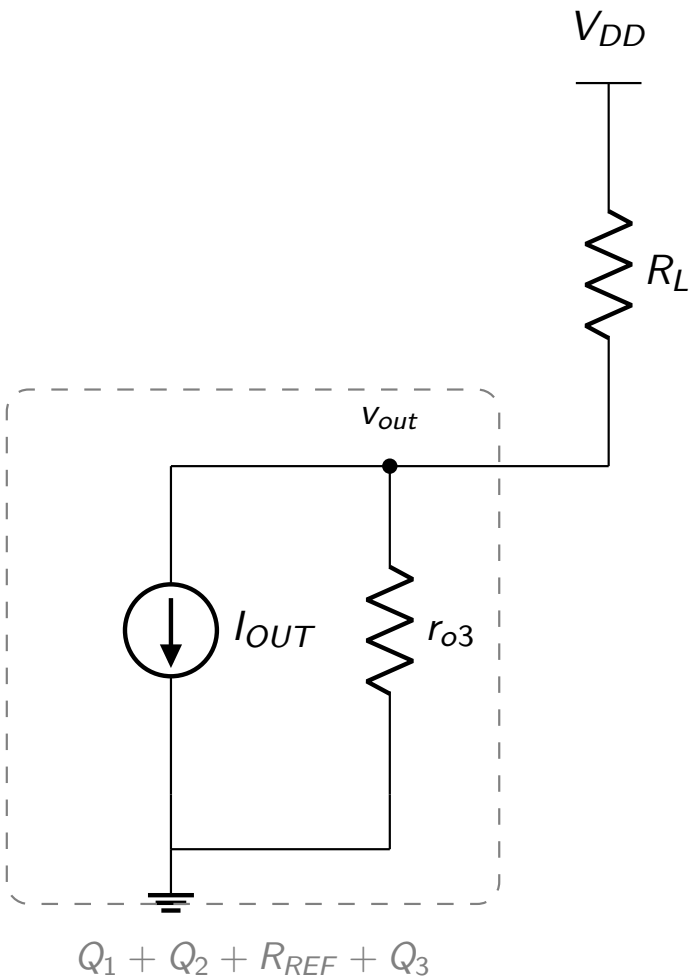
$$v_b \approx 0 \quad \Rightarrow \quad v_{be} = v_b - v_e = 0 - 0 = 0$$

Since $v_{be} = 0$: $g_{m3}\, v_{be} = 0$ (open circuit), $i_b = v_{be}/r_\pi = 0$ (r_π irrelevant)

The circuit reduces to the **same result** as the MOSFET case:



Norton Equivalent of the BJT Current Mirror



Replace all three BJTs and R_{REF} with their Norton equivalent:

- **Current source:** $I_{OUT} = I_{REF} \cdot \dfrac{A_3}{A_1}$
- **Where:** $I_{REF} = \dfrac{V_{DD} - 1.4\,\text{V}}{R_{REF}}$
- **Output resistance:** $r_{o3} = \dfrac{V_A}{I_{OUT}}$
- **Load:** R_L connects to V_{DD}

Same Norton form as the MOSFET mirror!
Only the expressions for I_{OUT} and r_{o3} differ.

Key Takeaways

1. **Active load MOSFETs** (gate tied to drain) are always in saturation
2. **Two in series** form a voltage divider where V_{MID} depends on W/L ratios
3. **NMOS–NMOS:** $R = \sqrt{(W/L)_2/(W/L)_1}$, uses only k'_n
4. **PMOS–NMOS:** $R = \sqrt{K_{p2}/K_{n1}}$, PMOS must be wider ($k'_p < k'_n$)
5. **Absolute sizing** controls current and power; **relative sizing** controls voltage
6. **Current mirror:** A second transistor sharing V_{GS} with the diode-connected device copies the current, scaled by $(W/L)_3/(W/L)_1$

Next: Current mirrors as active loads in amplifier circuits.