EE461g: Introduction to Electronic Circuits

Lecture 17

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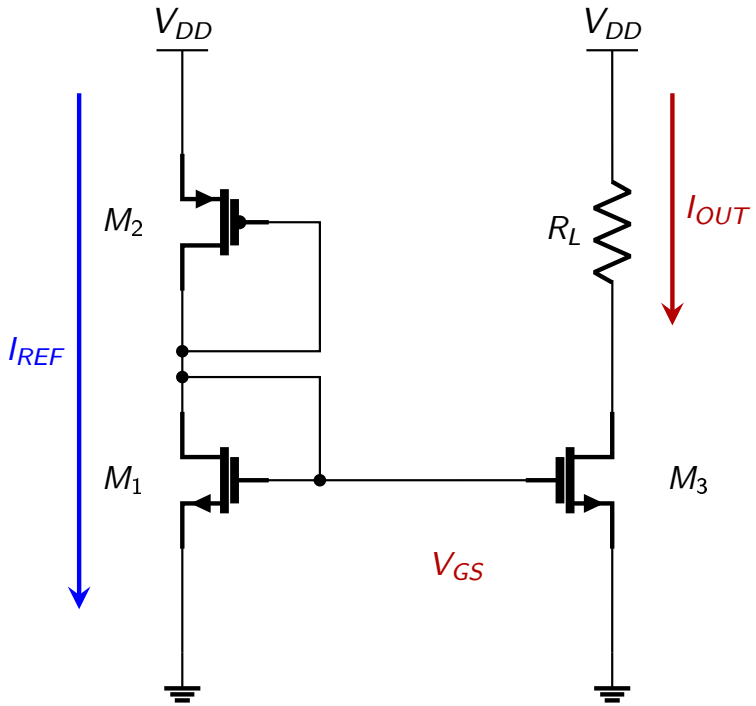
Outline

Review

The NMOS Current Mirror from Lecture 16

Recap: How the NMOS Mirror Works



From Lecture 16:

M_2 (PMOS) and M_1 (NMOS) are diode-connected, forming a bias network that sets V_{GS} and I_{REF}

M_3 shares the same V_{GS} as M_1

The current ratio:

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_3}{(W/L)_1}$$

Norton equivalent: I_{OUT} in parallel with r_{o3}

Today: What if we need more than one copy of the current?

Multiple NMOS Current Mirrors

One bias, many currents

The Key Insight: V_{GS} Is Just a Voltage

The diode-connected pair (M_2, M_1) creates a stable V_{GS} at the gate of M_1.

This V_{GS} is a **voltage** — it can drive more than one gate

Every NMOS whose gate is tied to this node sees the **same** V_{GS}

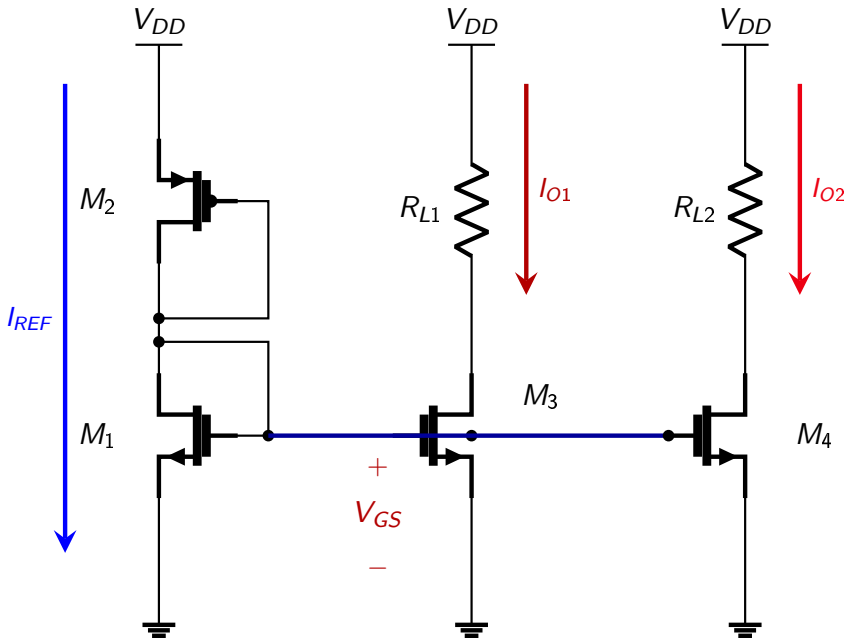
Each transistor independently produces:

$$I_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2$$

The only thing that differs between mirrors is their W/L ratio

One bias network $\rightarrow$ one V_{GS} $\rightarrow$ as many current copies as we want.

Adding a Second Mirror Transistor



Both M_3 and M_4 have their gates tied to the same V_{GS} node:

$$I_{O1} = I_{REF} \cdot \frac{(W/L)_3}{(W/L)_1}$$

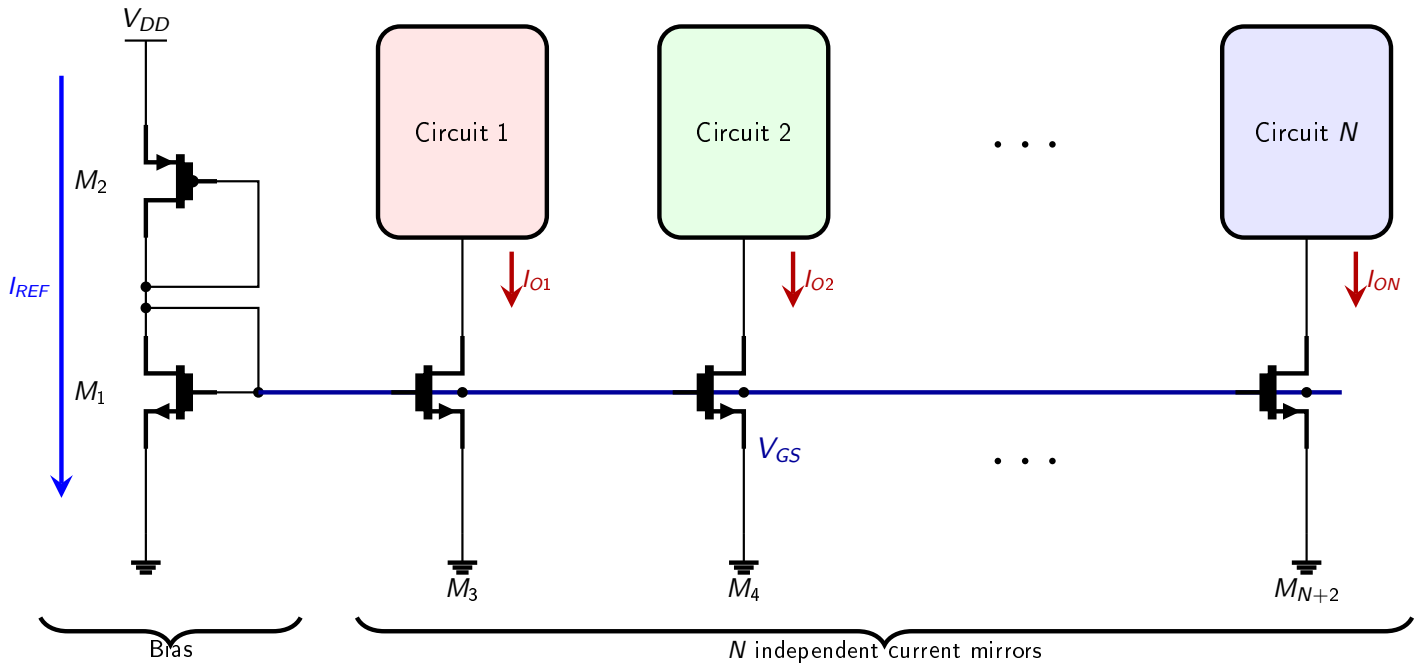
$$I_{O2} = I_{REF} \cdot \frac{(W/L)_4}{(W/L)_1}$$

Each mirror transistor:

- Sees the same V_{GS}
- Produces a current set by its own W/L
- Drives its own independent load
- Must remain in **saturation**

M_3 and M_4 don't interact — each is an independent current source.

Extending to N Mirror Transistors



Each output current is independently set:

$$I_{Ok} = I_{REF} \cdot \frac{(W/L)_k}{(W/L)_1} \qquad \text{for } k = 3, 4, \ldots, N+2$$

One bias pair generates I_{REF}. Every mirror transistor taps into the same V_{GS} and delivers its own current to its own circuit.

PMOS Current Mirror

Sourcing current from V_{DD}

NMOS Sinks, PMOS Sources

NMOS mirror (Lecture 16)

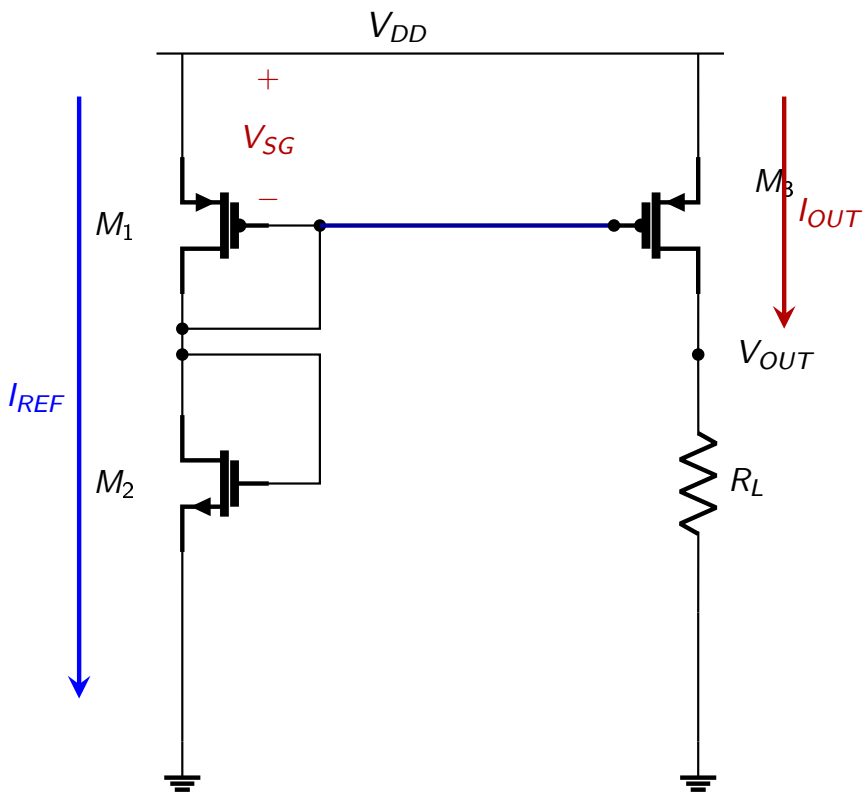
- Source tied to **ground**
- Current flows **into** the drain (sinks current down)
- The load connects between drain and V_{DD}
- Mirror sits **below** the load

PMOS mirror (today)

- Source tied to V_{DD}
- Current flows **out of** the drain (sources current down)
- The load connects between drain and ground
- Mirror sits **above** the load

NMOS mirrors **sink** current (pull to ground).
PMOS mirrors **source** current (limit what reaches R_L from V_{DD}).
Both are set by the same V_{GS} sharing principle.

PMOS Current Mirror Circuit



M_1 (PMOS) and M_2 (NMOS) are both diode-connected, forming the bias network that sets V_{SG} and I_{REF}.

M_3 shares the same V_{SG} as M_1:

$$V_{SG3} = V_{SG1}$$

So M_3 mirrors the current:

$$\boxed{\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_3}{(W/L)_1}}$$

Same mirror equation as NMOS — just using V_{SG} instead of V_{GS}.

PMOS Mirror: Deriving I_{OUT}

Both M_1 and M_3 are in saturation with $V_{SG1} = V_{SG3} = V_{SG}$.

For M_1 (diode-connected):

$$I_{REF} = \frac{k'_p}{2}\left(\frac{W}{L}\right)_1 (V_{SG} - |V_{TP}|)^2$$

For M_3 (mirror):

$$I_{OUT} = \frac{k'_p}{2}\left(\frac{W}{L}\right)_3 (V_{SG} - |V_{TP}|)^2$$

Taking the ratio:

$$\boxed{\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_3}{(W/L)_1}}$$

Identical derivation to the NMOS mirror. The $V_{SG} - |V_{TP}|$ terms cancel in the ratio, just as $V_{GS} - V_{TN}$ did for NMOS.

PMOS Mirror: Output Resistance

With channel-length modulation ($\lambda \neq 0$):

$$I_{OUT} = \frac{K_{p3}}{2}(V_{SG} - |V_{TP}|)^2(1 + \lambda V_{SD3})$$

The small-signal output resistance looking into the drain of M_3:

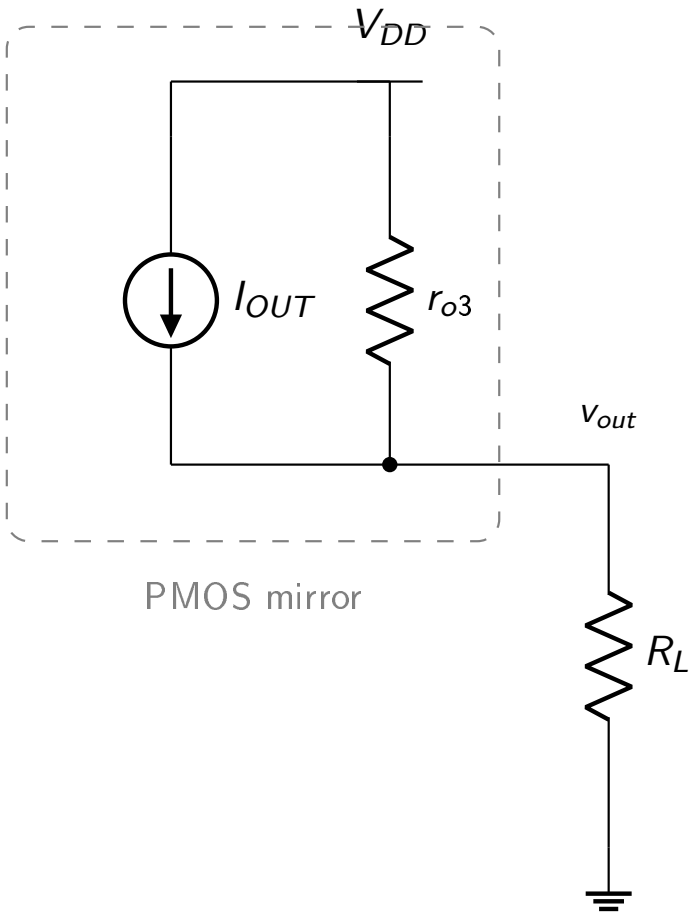
$$\boxed{r_{o3} = \frac{1}{\lambda I_{OUT}} = \frac{V_A}{I_{OUT}}}$$

This is the same form as the NMOS mirror:

	NMOS mirror	**PMOS mirror**
Current ratio	$(W/L)_3/(W/L)_1$	$(W/L)_3/(W/L)_1$
Output resistance	$r_{o3} = 1/(\lambda I_{OUT})$	$r_{o3} = 1/(\lambda I_{OUT})$

The Norton equivalent is the same form: I_{OUT} in parallel with r_{o3}. Only the direction of current flow differs.

Norton Equivalent of the PMOS Mirror



The PMOS mirror Norton equivalent:

Current source:

$$I_{OUT} = I_{REF} \cdot \frac{(W/L)_3}{(W/L)_1}$$

Output resistance:

$$r_{o3} = \frac{1}{\lambda I_{OUT}}$$

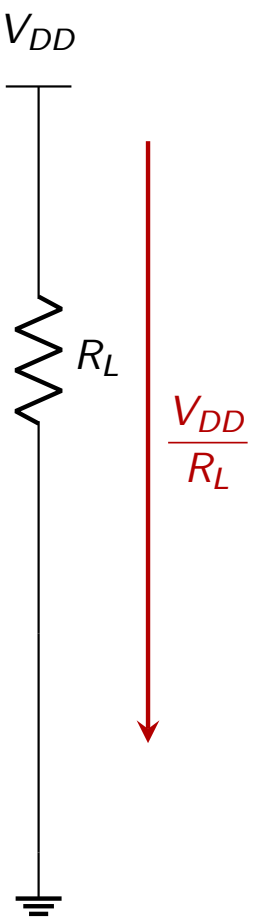
Load: R_L connects to ground

The PMOS mirror looks like an ideal current source I_{OUT} in parallel with r_{o3}, **holding back** current from reaching R_L.

PMOS Mirror Intuition

Holding current back from R_L

Without the PMOS Mirror



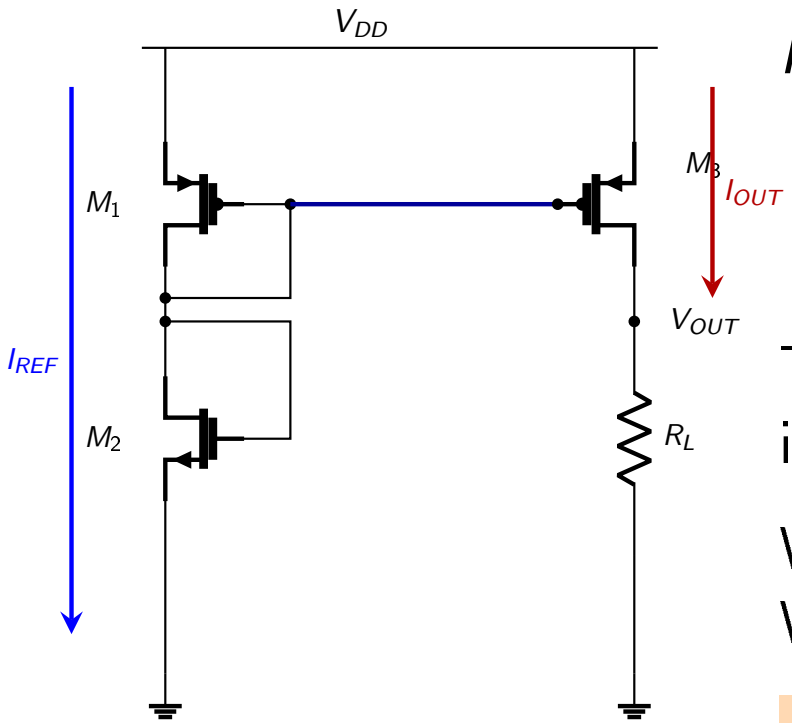
If R_L were connected directly between V_{DD} and ground:

$$I_{R_L} = \frac{V_{DD}}{R_L}$$

This is the **maximum** current that can flow through R_L.

Now we insert the PMOS mirror **between** V_{DD} **and** R_L...

With the PMOS Mirror: Holding Current Back



The PMOS mirror sits between V_{DD} and R_L, limiting the current to I_{OUT}:

$$I_{OUT} < \frac{V_{DD}}{R_L}$$

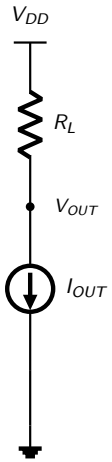
The PMOS is not *pushing* extra current into R_L — it is **holding it back**.

Without the mirror: $I = V_{DD}/R_L$
With the mirror: $I = I_{OUT} < V_{DD}/R_L$

The PMOS mirror restricts how much of V_{DD}'s current reaches R_L.

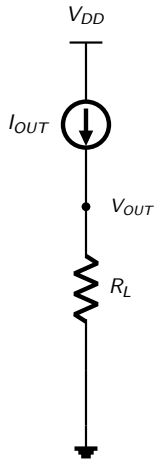
Same Story as the NMOS Mirror

NMOS mirror (Lec. 16)



Mirror below R_L.
Holds current back from flowing down through R_L to ground.

PMOS mirror (today)



Mirror above R_L.
Holds current back from reaching R_L from V_{DD}.

Both mirrors do the same thing: limit the current through R_L to I_{OUT}.
The only difference is whether the mirror sits above or below the load.

What If $V_{DD}/R_L < I_{OUT}$?

The PMOS mirror can only **limit** current, not **create** it.

If $\frac{V_{DD}}{R_L} < I_{OUT}$, the mirror tries to let through more current than R_L can carry at V_{DD}:

V_{OUT} rises toward V_{DD}

$V_{SD3} = V_{DD} - V_{OUT}$ shrinks

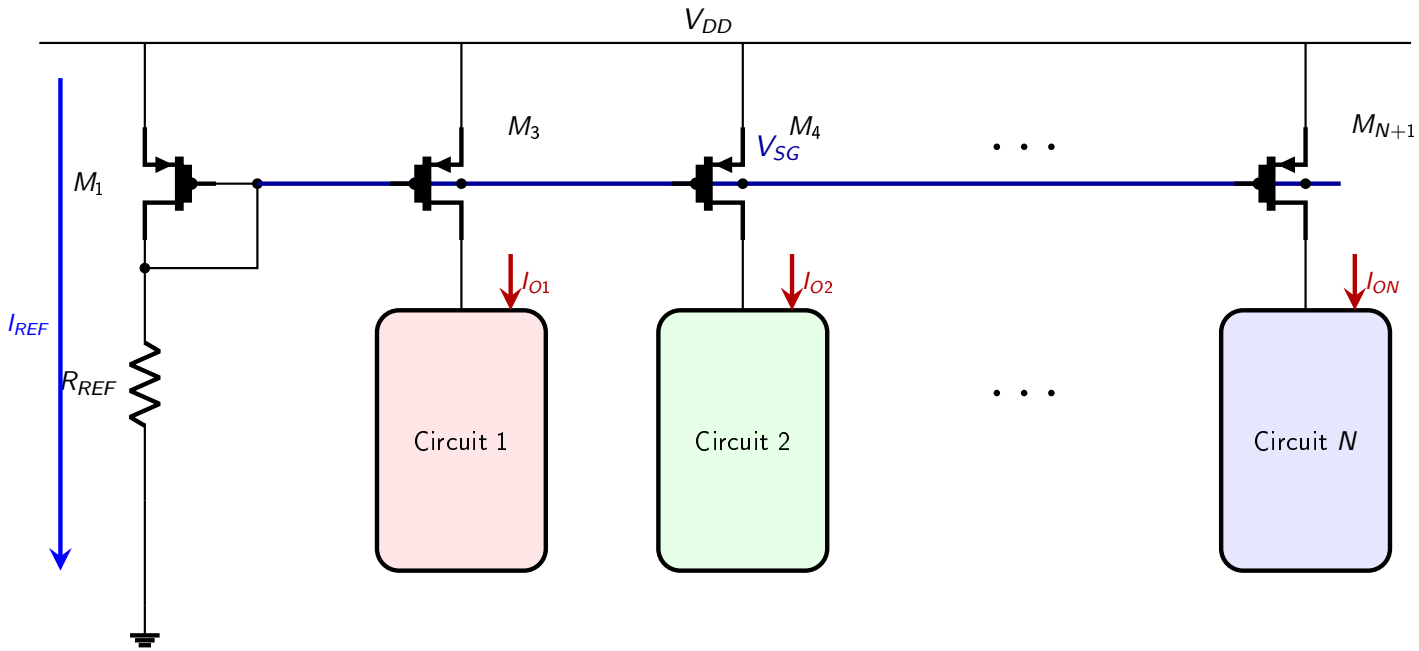
When $V_{SD3} < V_{SG} - |V_{TP}|$: M_3 leaves saturation $\rightarrow$ **triode region**

M_3 can no longer enforce I_{OUT} — the mirror breaks

The PMOS mirror works only when R_L is large enough that $\frac{V_{DD}}{R_L} > I_{OUT}$, keeping M_3 in saturation.

This is the mirror image of the NMOS condition from Lecture 16: there we needed R_L *small enough*; here we need R_L *large enough*.

PMOS Mirrors Can Also Fan Out



$$I_{Ok} = I_{REF} \cdot \frac{(W/L)_k}{(W/L)_1} \qquad \text{for each PMOS mirror } M_k$$

Same fan-out idea as NMOS: one bias PMOS sets V_{SG}, and N mirror PMOS transistors each source current into their own circuit.

SPICE Simulation

How large can R_L get?

NMOS Mirror: SPICE Netlist

```
* NMOS Current Mirror - Sweep VDS of mirror transistor
VDD vdd 0 DC 5

* Bias pair (diode-connected)
M2 vmid vmid vdd vdd PMOS_BASIC W=10u L=1u
M1 vmid vmid 0   0   NMOS_BASIC W=10u L=1u

* Mirror transistor M3
M3 vout vmid 0 0 NMOS_BASIC W=10u L=1u

* Sweep drain voltage of M3 (= Vout)
* RL_effective = (VDD - Vout) / Id3
Vdrain vout 0 DC 0

.model NMOS_BASIC NMOS(VTO=0.7 KP=200u LAMBDA=0.02)
.model PMOS_BASIC PMOS(VTO=-0.7 KP=100u LAMBDA=0.02)

.dc Vdrain 0 5 0.01
```

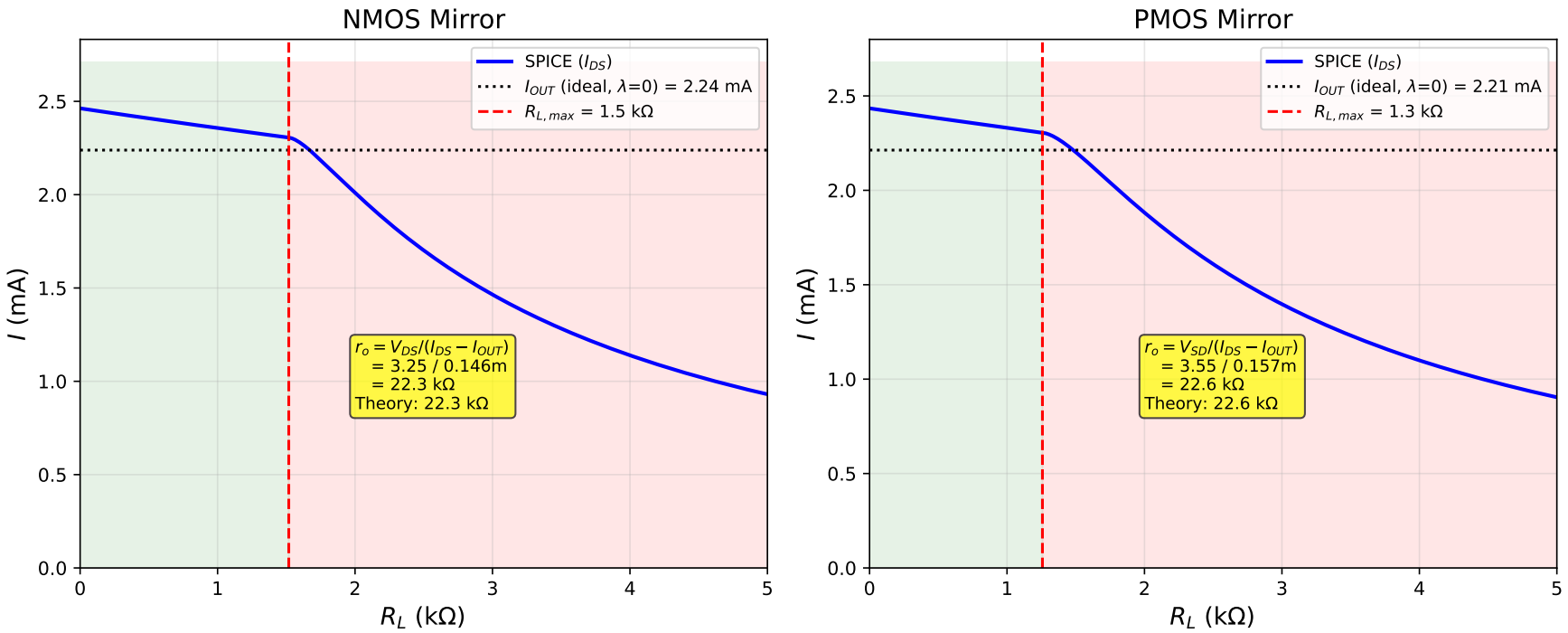
We sweep V_{OUT} (the drain voltage of M_3) from 0 to V_{DD}. At each point, the effective $R_L = (V_{DD} - V_{OUT})/I_{OUT}$. As R_L increases, V_{OUT} drops — when $V_{DS3} < V_{GS} - V_{TN}$, M_3 enters triode.

PMOS Mirror: SPICE Netlist

```
* PMOS Current Mirror - Sweep Vout of mirror transistor
VDD vdd 0 DC 5

* Bias pair (diode-connected)
M1 vmid vmid vdd vdd PMOS_BASIC W=10u L=1u
M2 vmid vmid 0   0   NMOS_BASIC W=10u L=1u

* Mirror transistor M3 (PMOS)
M3 vout vmid vdd vdd PMOS_BASIC W=10u L=1u

* Sweep drain voltage of M3 (= Vout)
* RL_effective = Vout / |Id3|
Vdrain vout 0 DC 0

.model NMOS_BASIC NMOS(VTO=0.7 KP=200u LAMBDA=0.02)
.model PMOS_BASIC PMOS(VTO=-0.7 KP=100u LAMBDA=0.02)

.dc Vdrain 0 5 0.01
```

Same idea, but now the PMOS mirror sits above R_L. As R_L increases, V_{OUT} rises — when $V_{SD3} < V_{SG} - |V_{TP}|$, M_3 enters triode.

SPICE Results: I_{OUT} vs R_L



In the **green** region (saturation), I_{OUT} is *not* perfectly constant — it has a slight slope due to channel-length modulation ($\lambda \neq 0$).

In the **red** region (triode), I_{OUT} drops sharply — the mirror can no longer hold current back.

NMOS: $R_{L,max} \approx 1.5\,\text{k}\Omega$ **PMOS:** $R_{L,max} \approx 1.3\,\text{k}\Omega$

Extracting r_o from the Norton Equivalent

From the Norton equivalent, the total drain current is $I_{DS} = I_{OUT} + V_{DS}/r_o$, where I_{OUT} is the ideal current ($\lambda = 0$) and the extra current flows through r_o. Solving:

$$r_o = \frac{V_{DS}}{I_{DS} - I_{OUT}}$$

	I_{OUT} (λ=0)	I_{DS} (SPICE)	$r_o = V_{DS}/(I_{DS} - I_{OUT})$	$1/\lambda I_{OUT}$
NMOS	2.24 mA	2.38 mA	22.3 kΩ	22.3 kΩ
PMOS	2.21 mA	2.37 mA	22.6 kΩ	22.6 kΩ

Exact match: $r_o = V_{DS}/(I_{DS} - I_{OUT}) = 1/(\lambda\, I_{OUT})$.
The dotted line on the plot shows I_{OUT} — the gap above it is $I_{r_o} = V_{DS}/r_o$.

Why the $R_{L,max}$ Limits Differ

Both mirrors use $V_{DD} = 5$ V, $V_{TN} = 0.7$ V, $|V_{TP}| = 0.7$ V, $W/L = 10$.

NMOS mirror (M_3 below R_L):

$$V_{DS3,min} = V_{GS} - V_{TN} = 2.20 - 0.7 = 1.50 \text{ V}$$
$$R_{L,max} = \frac{V_{DD} - V_{DS3,min}}{I_{OUT}} = \frac{3.50}{2.35 \text{ mA}} \approx 1.5 \text{ k}\Omega$$

PMOS mirror (M_3 above R_L):

$$V_{SD3,min} = V_{SG} - |V_{TP}| = 2.80 - 0.7 = 2.10 \text{ V}$$
$$R_{L,max} = \frac{V_{DD} - V_{SD3,min}}{I_{OUT}} = \frac{2.90}{2.32 \text{ mA}} \approx 1.3 \text{ k}\Omega$$

The PMOS needs more headroom ($V_{SD,sat}$ is larger because $k_p' < k_n'$ forces a larger V_{SG}), so its $R_{L,max}$ is smaller.

Key Takeaways

A single bias pair creates a V_{GS} that can drive **any number** of mirror transistors

Each mirror produces $I_{Ok} = I_{REF} \cdot (W/L)_k/(W/L)_1$, independently

PMOS mirrors use V_{SG} — same mirror equation, same Norton form

Both NMOS and PMOS mirrors **hold current back** — they limit, not push

The mirror works only while the transistor stays in **saturation**

$R_{L,max}$ is set by how much voltage headroom the mirror transistor needs