EE461g: Introduction to Electronic Circuits

Lecture 18

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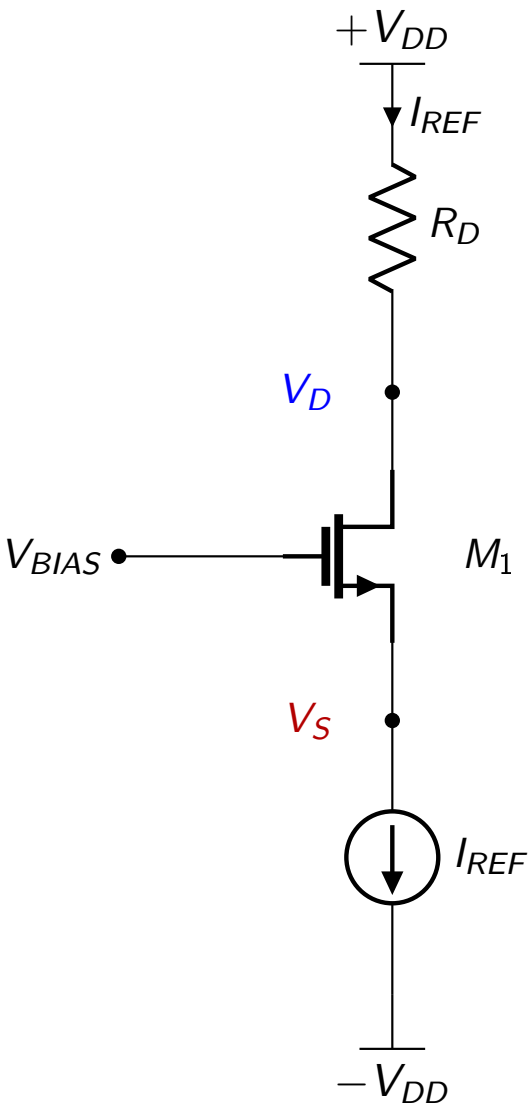
Outline

1. NMOS with Current Source Biasing
2. Finding the Source Voltage V_S
3. Finding the Drain Voltage V_D
4. Verifying Saturation
5. Maximum V_{BIAS} for Saturation
6. Summary
7. MOSFET Current Mirror Implementation
8. Minimum V_{BIAS} for M_4 Saturation
9. The Differential Pair
10. BJT Differential Pair
11. Summary

NMOS Biasing

with a Current Source

The Circuit



Circuit description:

$+V_{DD}$ supplies current through R_D to the drain

Gate is held at a fixed DC voltage V_{BIAS}

A current source I_{REF} is connected from the source to $-V_{DD}$

The current source **fixes** $I_D = I_{REF}$

Goal: Find V_D and V_S

Finding V_S

The Source Voltage

Step 1: Assume Saturation

We assume M_1 operates in **saturation**. We will verify this at the end.

In saturation, the drain current is:

$$I_D = \frac{k'_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2$$

Since the current source fixes $I_D = I_{REF}$:

$$\boxed{I_{REF} = \frac{k'_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2}$$

The current is **known**. We can solve this equation for V_{GS}.

Step 2: Solve for V_{GS}

Starting from: $I_{REF} = \frac{k'_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2$

Isolate the squared term: $(V_{GS} - V_{TN})^2 = \frac{2I_{REF}}{k'_n(W/L)}$

Take the square root (positive root since $V_{GS} > V_{TN}$ in saturation):

$$V_{GS} - V_{TN} = \sqrt{\frac{2I_{REF}}{k'_n(W/L)}}$$

$$\boxed{V_{GS} = V_{TN} + \sqrt{\frac{2I_{REF}}{k'_n(W/L)}}}$$

V_{GS} depends only on the current I_{REF}, transistor parameters, and V_{TN}.

Step 3: Extract V_S from V_{GS}

By definition:

$$V_{GS} = V_G - V_S$$

Since $V_G = V_{BIAS}$:

$$V_S = V_G - V_{GS} = V_{BIAS} - V_{GS}$$

Substituting our expression for V_{GS}:

$$\boxed{V_S = V_{BIAS} - V_{TN} - \sqrt{\frac{2I_{REF}}{k'_n(W/L)}}}$$

V_S is completely determined by V_{BIAS}, the current source I_{REF}, and transistor parameters.

Finding V_D

The Drain Voltage

Step 4: Apply KVL Through R_D

The current through R_D is $I_D = I_{REF}$ (set by the current source I_{REF}).

Applying KVL from $+V_{DD}$ through R_D to the drain:

$$V_D = V_{DD} - I_D \cdot R_D$$

Since $I_D = I_{REF}$:

$$\boxed{V_D = V_{DD} - I_{REF} \cdot R_D}$$

V_D depends only on V_{DD}, the current I_{REF}, and R_D. It does not depend on transistor parameters!

Verifying

Saturation Condition

Step 5: Check the Saturation Condition

For an NMOS in saturation, we need:

$$V_{DS} \geq V_{GS} - V_{TN} \quad \text{(equivalently, } V_D \geq V_G - V_{TN})$$

We can compute V_{DS}:

$$V_{DS} = V_D - V_S = (V_{DD} - I_{REF} R_D) - \left(V_{BIAS} - V_{TN} - \sqrt{\frac{2I_{REF}}{k'_n(W/L)}} \right)$$

And the overdrive voltage is:

$$V_{OV} = V_{GS} - V_{TN} = \sqrt{\frac{2I_{REF}}{k'_n(W/L)}}$$

Check: $V_{DS} \geq V_{OV}$. If yes, our saturation assumption is valid.

Maximum V_{BIAS}

Keeping the MOSFET in Saturation

Step 6: Set Up the Saturation Inequality

The saturation condition requires:

$$V_{DS} \geq V_{GS} - V_{TN}$$

Rewrite using $V_{DS} = V_D - V_S$:

$$V_D - V_S \geq V_{GS} - V_{TN}$$

Since $V_{GS} = V_G - V_S = V_{BIAS} - V_S$, substituting:

$$V_D - V_S \geq V_{BIAS} - V_S - V_{TN}$$

The V_S terms cancel:

$$V_D \geq V_{BIAS} - V_{TN}$$

The saturation condition simplifies to a constraint on V_D and V_{BIAS} only.

Step 7: Substitute V_D and Solve for V_{BIAS}

Substitute $V_D = V_{DD} - I_{REF} \cdot R_D$:

$$V_{DD} - I_{REF} \cdot R_D \geq V_{BIAS} - V_{TN}$$

Rearrange to isolate V_{BIAS}:

$$V_{BIAS} \leq V_{DD} - I_{REF} \cdot R_D + V_{TN}$$

Therefore the maximum value of V_{BIAS} is:

$$\boxed{V_{BIAS,\text{max}} = V_{DD} - I_{REF} \cdot R_D + V_{TN}}$$

If V_{BIAS} exceeds this value, the MOSFET enters the **triode** (linear) region and the current source can no longer set $I_D = I_{REF}$.

Interpretation

$$V_{BIAS,\max} = \underbrace{V_{DD} - I_{REF} \cdot R_D}_{V_D} + V_{TN}$$

$V_{BIAS,\max}$ equals the drain voltage plus one threshold voltage

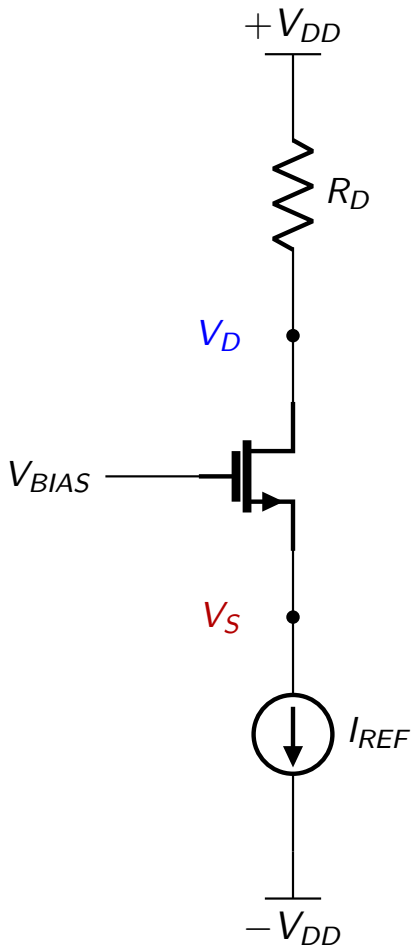
Increasing V_{BIAS} beyond this pushes $V_{GS} - V_{TN}$ above V_{DS} — the transistor leaves saturation

Larger $R_D \rightarrow$ larger voltage drop $\rightarrow$ lower $V_D \rightarrow$ lower $V_{BIAS,\max}$

Larger $I_{REF} \rightarrow$ same effect: lower $V_D \rightarrow$ lower $V_{BIAS,\max}$

Design trade-off: A larger R_D gives more voltage gain but restricts the allowable range of V_{BIAS}.

Summary of Results



Source voltage:

$$V_S = V_{BIAS} - V_{TN} - \sqrt{\frac{2I_{REF}}{k_n'(W/L)}}$$

Drain voltage:

$$V_D = V_{DD} - I_{REF} \cdot R_D$$

Max V_{BIAS} for saturation:

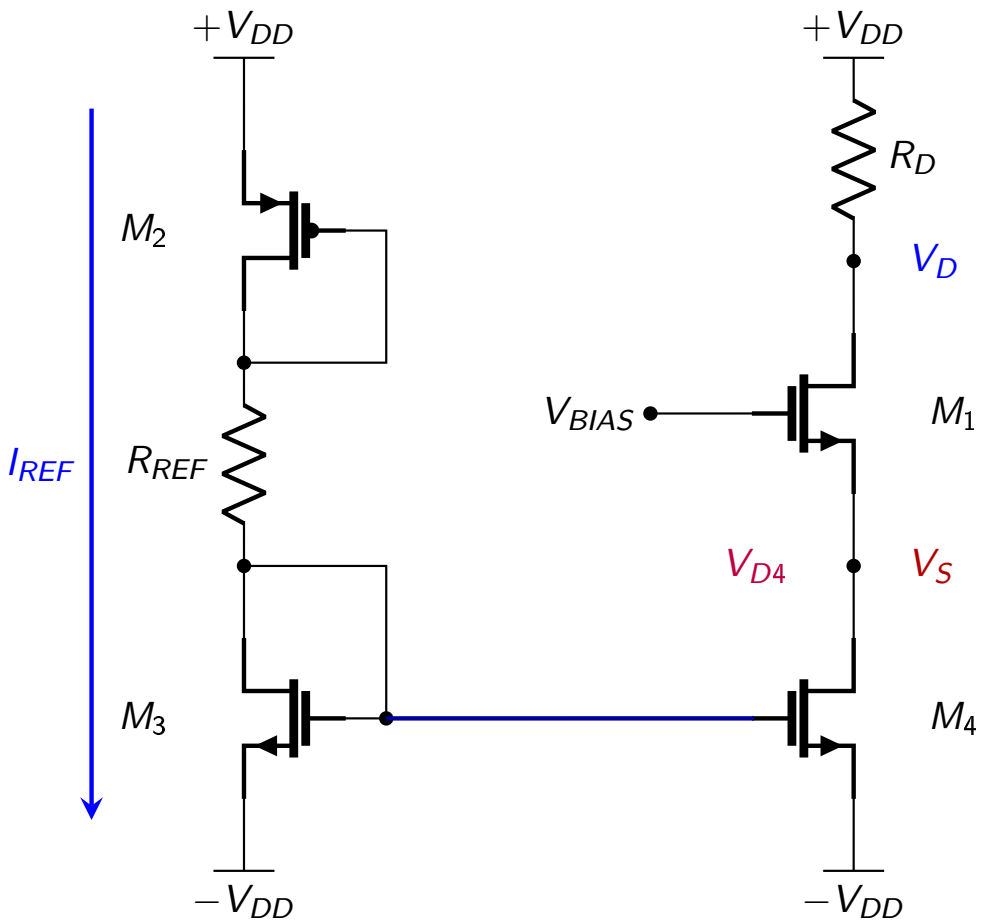
$$V_{BIAS,\max} = V_{DD} - I_{REF} \cdot R_D + V_{TN}$$

The current source makes I_D independent of V_{BIAS} drift — but V_{BIAS} must stay below $V_{BIAS,\max}$.

Replacing the Ideal Current Source

PMOS + NMOS Current Mirror from Lecture 16

The Complete Circuit



Circuit Description

Left side (bias network):

M_2 (PMOS, diode-connected), R_{REF}, and M_3 (NMOS, diode-connected) set I_{REF}

$$I_{REF} = \frac{2V_{DD} - |V_{GS2}| - V_{GS3}}{R_{REF}}$$

Right side:

M_4 mirrors I_{REF} from M_3 (same V_{GS})

Current ratio: $I_D = I_{REF} \cdot \frac{(W/L)_4}{(W/L)_3}$

M_4 replaces the ideal current source under M_1

M_1 is biased by V_{BIAS} at the gate

All previous results for V_D, V_S, and $V_{BIAS,\text{max}}$ still hold — but now we must also keep M_4 in **saturation**.

Circuit Parameters

Supplies:

$$V_{DD} = 5\,\text{V},\ -V_{DD} = -5\,\text{V}$$

Resistors:

$$R_D = 1\,\text{k}\Omega$$

$$R_{REF} = 80\,\text{k}\Omega$$

MOSFET Models:

$$k_n' = 1600\,\mu\text{A/V}^2,$$
$$k_p' = 800\,\mu\text{A/V}^2$$

$$V_{TN} = 0.5\,\text{V}, \quad V_{TP} = -0.5\,\text{V}$$

$$\lambda = 0.02\,\text{V}^{-1}$$

Transistor Sizing:

	W/L	Role
M_1	0.5	Amplifier
M_2	1.0	PMOS bias
M_3	0.5	NMOS bias
M_4	0.5	Mirror

Operating point ($V_{BIAS} = 0$):

$$I_{REF} \approx 100\,\mu\text{A}$$

$$V_{GS} \approx 1.0\,\text{V}$$

$$V_S \approx -1.0\,\text{V}$$

$$V_D \approx 4.9\,\text{V}$$

Minimum V_{BIAS}

Keeping M_4 in Saturation

M_4 Saturation Condition

For NMOS M_4 to remain in **saturation**:

$$V_{DS4} \geq V_{GS4} - V_{TN} = V_{OV4}$$

The drain of M_4 is connected to the source of M_1, so $V_{D4} = V_S$.
The source of M_4 is connected to $-V_{DD}$, so:

$$V_{DS4} = V_{D4} - V_{S4} = V_S - (-V_{DD}) = V_S + V_{DD}$$

Since M_4 shares V_{GS} with diode-connected M_3 (both sources at $-V_{DD}$):

$$V_{OV4} = V_{GS4} - V_{TN} = \sqrt{\frac{2I_{REF}}{k'_n(W/L)_3}}$$

The saturation condition becomes:

$$\boxed{V_S + V_{DD} \geq V_{OV4}}$$

Solve for Minimum V_S

From the saturation condition:

$$V_S + V_{DD} \geq V_{OV4}$$

Solving for V_S:

$$V_S \geq V_{OV4} - V_{DD}$$

Now recall our expression for V_S:

$$V_S = V_{BIAS} - V_{TN} - V_{OV1}$$

where $V_{OV1} = \sqrt{\frac{2I_{REF}}{k'_n(W/L)_1}}$ is the overdrive of M_1.

Substituting:

$$V_{BIAS} - V_{TN} - V_{OV1} \geq V_{OV4} - V_{DD}$$

This places a **lower bound** on V_{BIAS}.

Solve for Minimum V_{BIAS}

Rearranging:

$$V_{BIAS} \geq V_{OV4} - V_{DD} + V_{TN} + V_{OV1}$$

Recognizing that $V_{TN} + V_{OV1} = V_{GS1}$:

$$\boxed{V_{BIAS,\text{min}} = V_{OV4} - V_{DD} + V_{GS1}}$$

where:

$$V_{OV4} = \sqrt{\frac{2I_{REF}}{k'_n(W/L)_3}} \text{ — overdrive of the mirror transistor } M_4$$

$$V_{GS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{k'_n(W/L)_1}} \text{ — gate-source voltage of } M_1$$

If V_{BIAS} drops below this value, M_4 enters **triode** and can no longer mirror I_{REF} accurately.

The Allowable Range of V_{BIAS}

Combining both constraints:

$$\boxed{V_{OV4} - V_{DD} + V_{GS1} \leq V_{BIAS} \leq V_{DD} - I_{REF} \cdot R_D + V_{TN}}$$

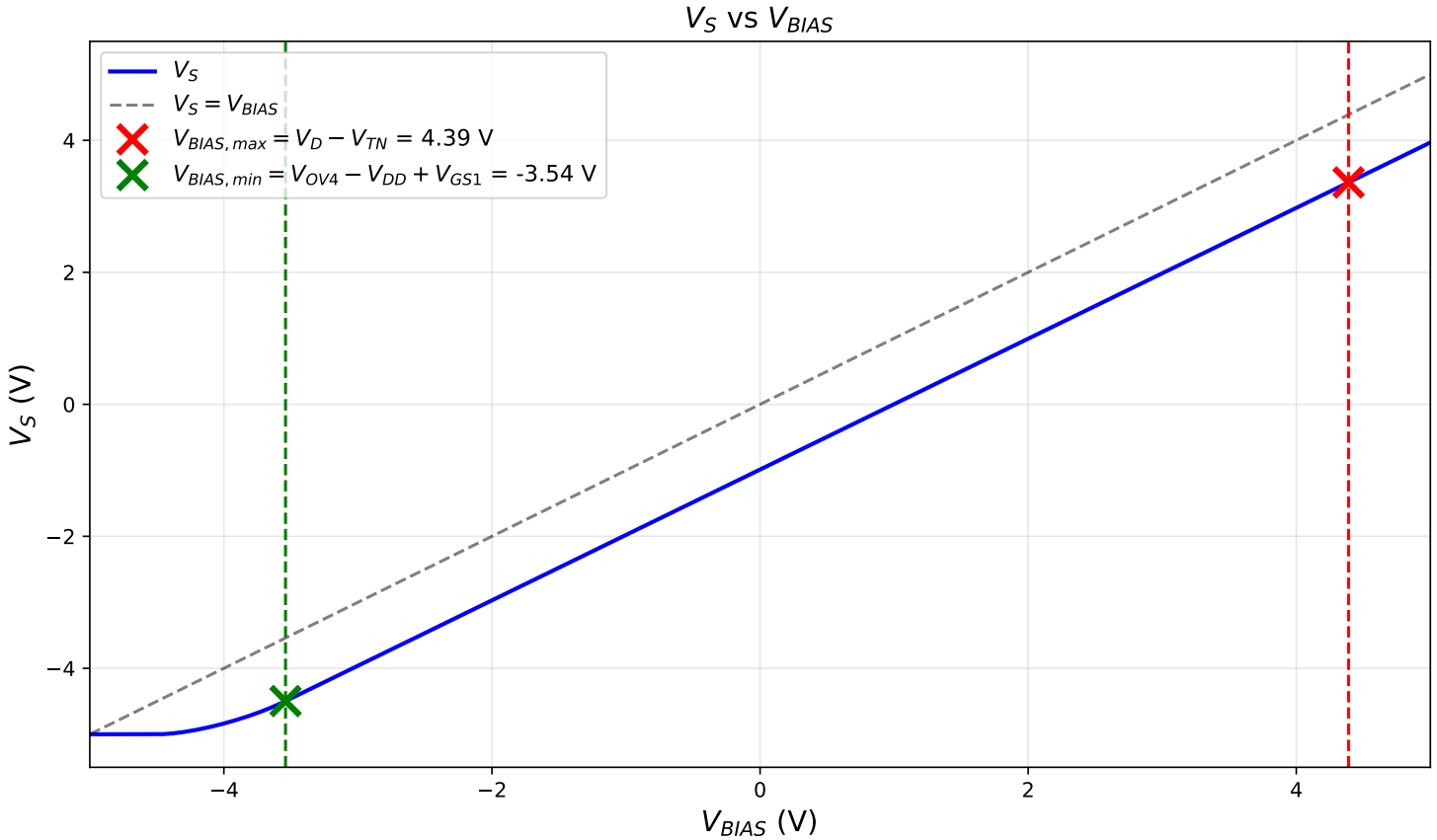
$$V_{BIAS,\text{min}} \leq V_{BIAS} \leq V_{BIAS,\text{max}}$$

Upper limit (from M_1 saturation): $V_{BIAS,\text{max}} = V_D + V_{TN}$

Lower limit (from M_4 saturation):
$V_{BIAS,\text{min}} = V_{OV4} - V_{DD} + V_{GS1}$

Both M_1 and the mirror transistor M_4 must remain in saturation for the circuit to function correctly.

SPICE Simulation: V_S vs V_{BIAS}

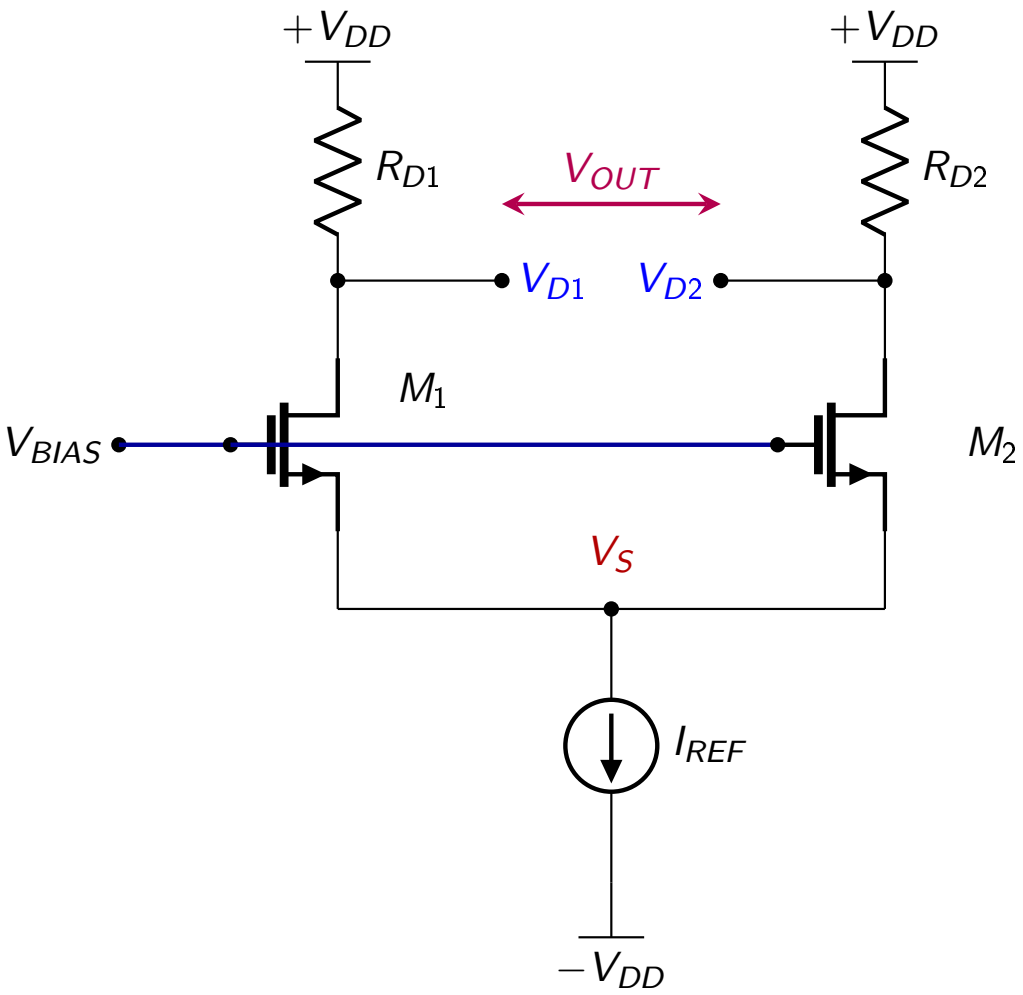


V_S tracks V_{BIAS} linearly in saturation. Red X marks $V_{BIAS} = V_D - V_{TN}$ — beyond this, M_1 enters triode.

The Differential Pair

Two MOSFETs Sharing One Current Source

The Differential Pair Circuit



The Differential Pair

Both gates tied to V_{BIAS} — this is the **bias point** of a differential pair

Each transistor has its own drain resistor (R_{D1}, R_{D2})

Sources tied together at V_S; current source sinks $I_{REF} = I_{D1} + I_{D2}$

With matched transistors and $V_{G1} = V_{G2}$, the current splits equally:

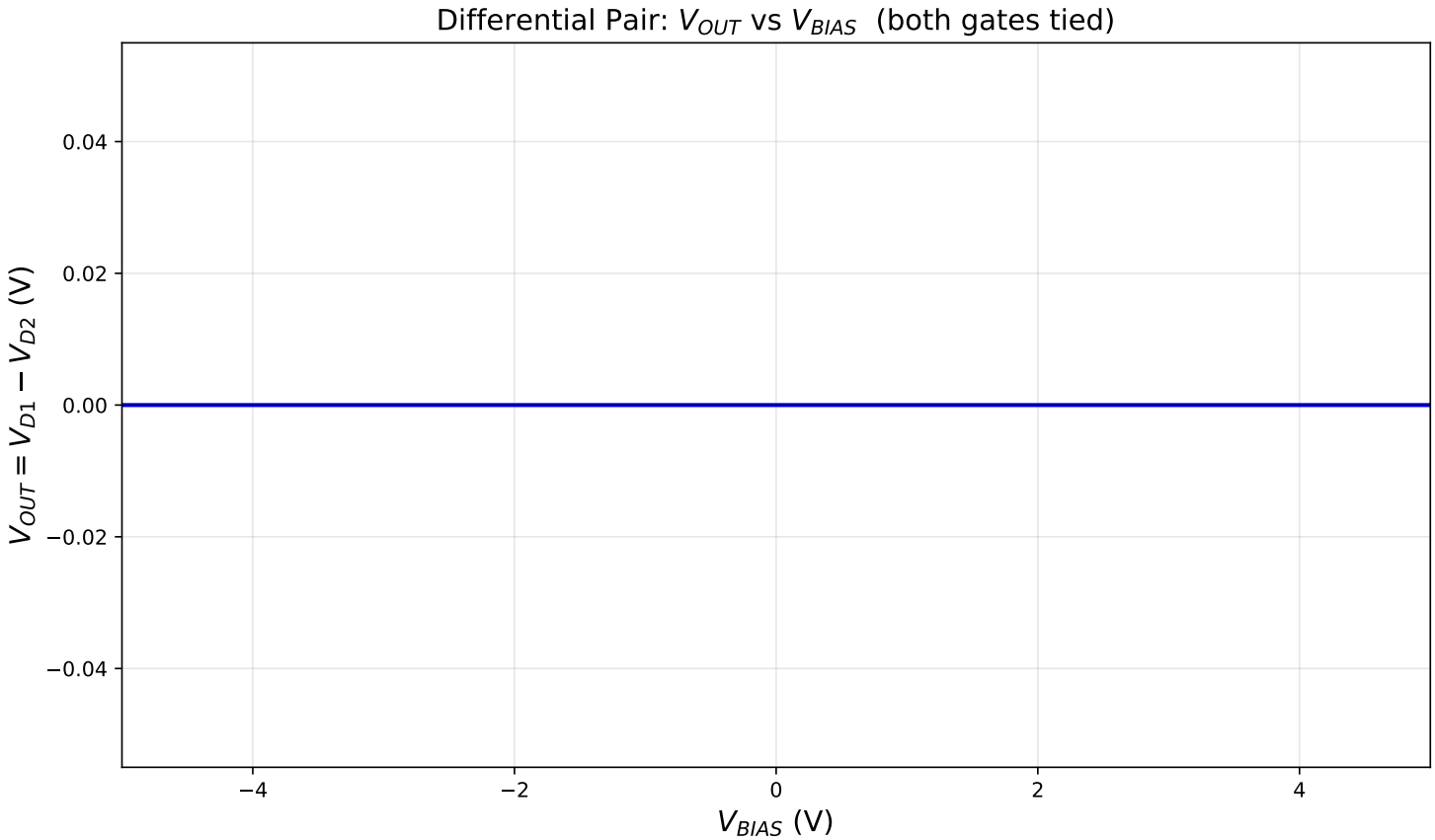
$$I_{D1} = I_{D2} = \frac{I_{REF}}{2}$$

The drain voltages are:

$$V_{D1} = V_{DD} - \frac{I_{REF}}{2} \cdot R_{D1}, \qquad V_{D2} = V_{DD} - \frac{I_{REF}}{2} \cdot R_{D2}$$

This is the foundation of the **differential amplifier**. Next step: apply different voltages to each gate and see how the current steers.

SPICE Simulation: V_{OUT} vs V_{BIAS}

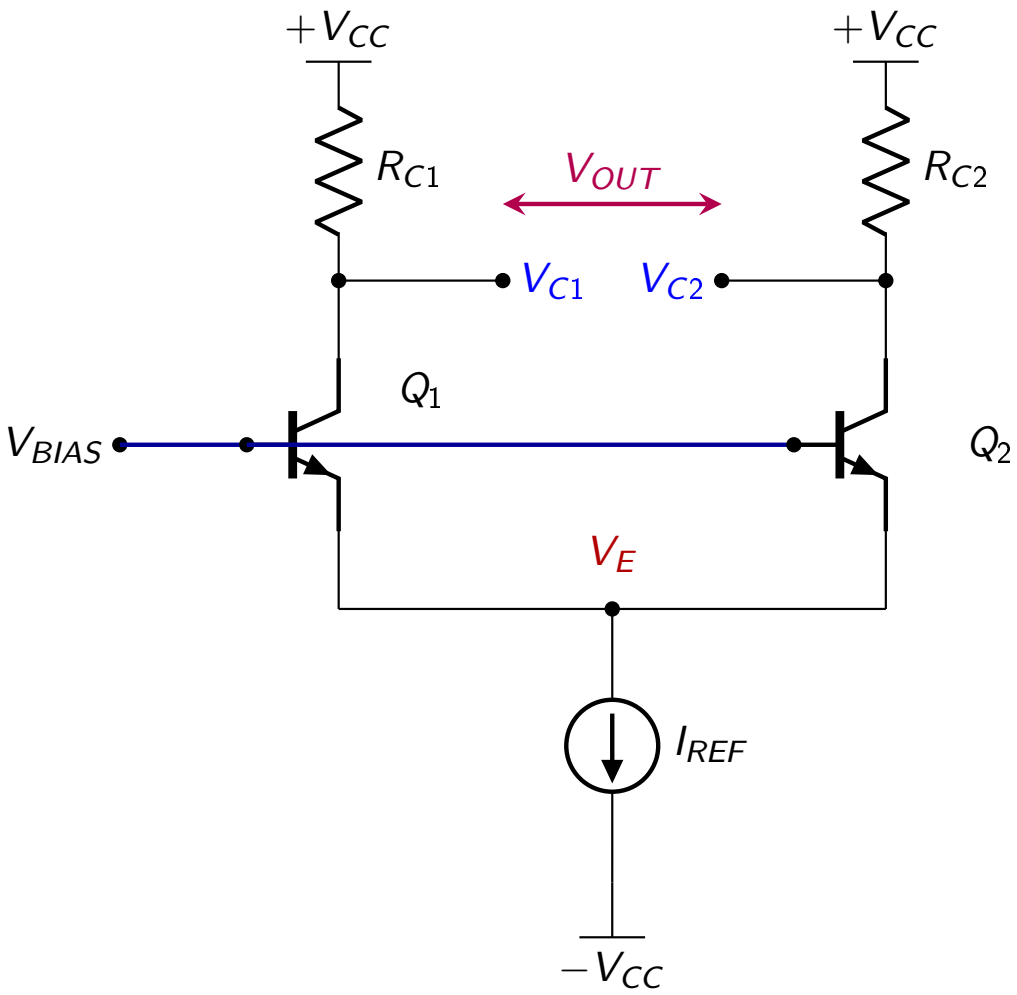


With both gates tied to V_{BIAS}, $V_{OUT} = V_{D1} - V_{D2} = 0$ for all V_{BIAS}.
Matched transistors split I_{REF} equally — no differential output.

BJT Differential Pair

Same Analysis, Different Device

The BJT Differential Pair Circuit



The BJT Differential Pair

Both bases tied to V_{BIAS} — identical to the MOSFET case

Each transistor has its own collector resistor (R_{C1}, R_{C2})

Emitters tied together at V_E; current source sinks $I_{REF} = I_{C1} + I_{C2}$

With matched transistors and $V_{B1} = V_{B2}$, the current splits equally:

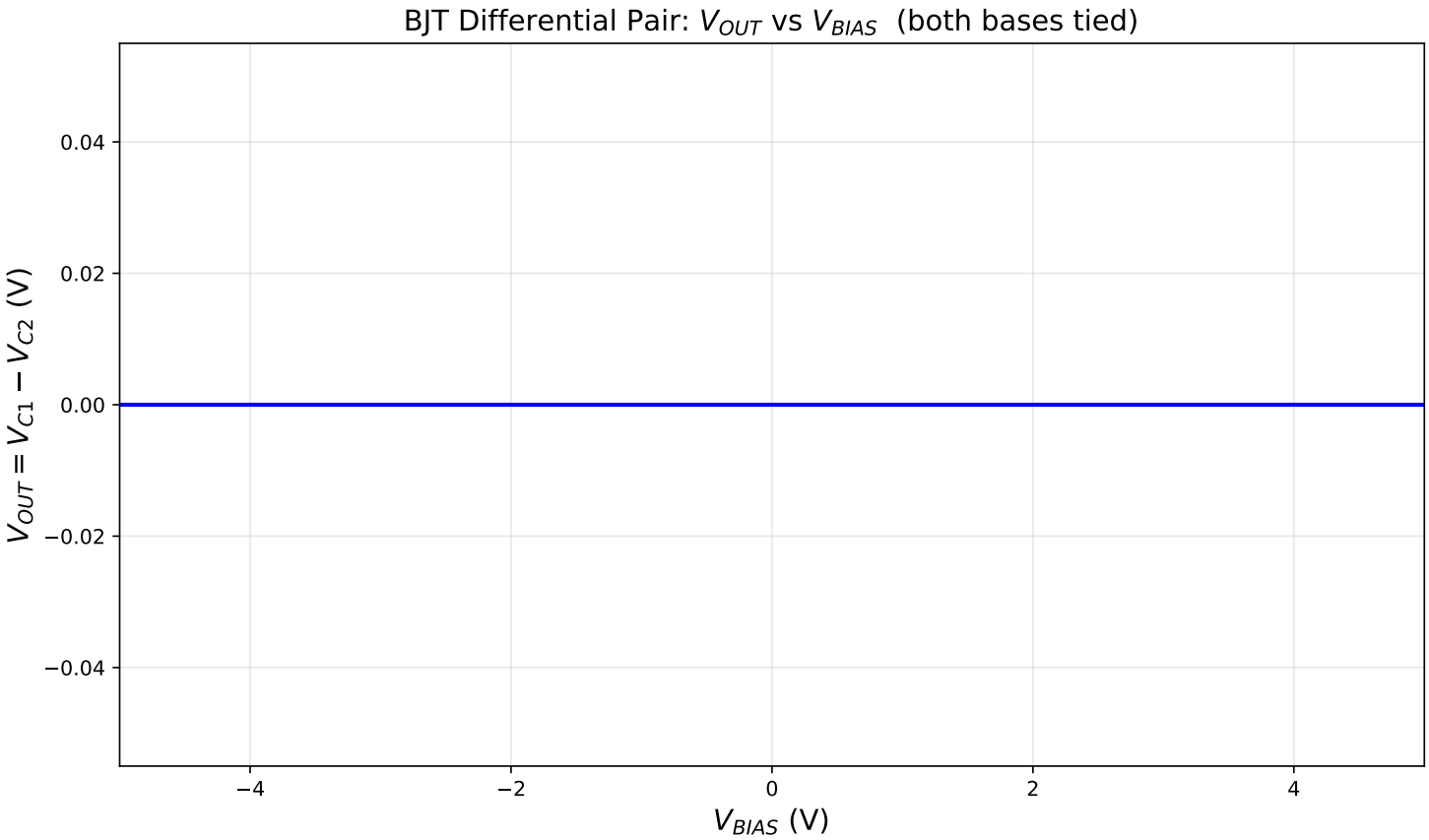
$$I_{C1} = I_{C2} = \frac{I_{REF}}{2}$$

The collector voltages are:

$$V_{C1} = V_{CC} - \frac{I_{REF}}{2} \cdot R_{C1}, \qquad V_{C2} = V_{CC} - \frac{I_{REF}}{2} \cdot R_{C2}$$

Key difference: BJT has $V_E = V_{BIAS} - V_{BE}$ (fixed ≈ 0.7 V drop) vs. MOSFET $V_S = V_{BIAS} - V_{GS}$ (depends on $\sqrt{I_D}$).

SPICE Simulation: BJT V_{OUT} vs V_{BIAS}



With both bases tied to V_{BIAS}, $V_{OUT} = V_{C1} - V_{C2} = 0$ for all V_{BIAS}. Matched transistors split I_{REF} equally — same result as the MOSFET pair.

Lecture 18 Summary

Single NMOS with current source biasing: $V_S = V_{BIAS} - V_{GS}$, $V_D = V_{DD} - I_{REF} \cdot R_D$

Maximum V_{BIAS} (keeping M_1 in saturation): $V_{BIAS,\max} = V_{DD} - I_{REF} \cdot R_D + V_{TN}$

MOSFET current mirror replaces the ideal current source:

PMOS + R_{REF} + NMOS bias network sets I_{REF}; mirror transistor copies the current

Minimum V_{BIAS} (keeping mirror in saturation): $V_{BIAS,\min} = V_{OV4} - V_{DD} + V_{GS1}$

MOSFET differential pair: two matched MOSFETs sharing a tail current source

With equal gate voltages: $I_{D1} = I_{D2} = I_{REF}/2$ and $V_{OUT} = 0$

BJT differential pair: same topology with NPN transistors

With equal base voltages: $I_{C1} = I_{C2} = I_{REF}/2$ and $V_{OUT} = 0$
Key difference: $V_E = V_{BIAS} - V_{BE}$ (fixed) vs. $V_S = V_{BIAS} - V_{GS}$ ($\sqrt{I_D}$-dependent)

Next: Apply different voltages to each gate/base and analyze current steering and differential gain.