EE461g: Introduction to Electronic Circuits

Lecture 19

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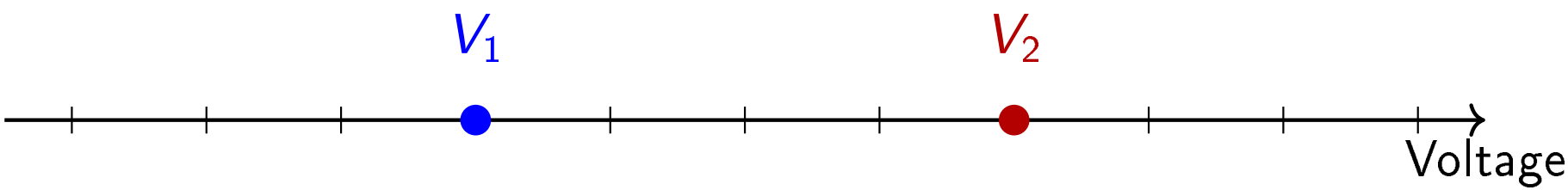
Outline

Decomposing Two Voltages

into Common-Mode and Differential

Two Input Voltages V_1 and V_2

Consider two voltages applied to the gates (or bases) of a differential pair:



We can describe these two voltages using two **new** quantities:

Common-mode voltage:

$$V_{CM} = \frac{V_1 + V_2}{2}$$

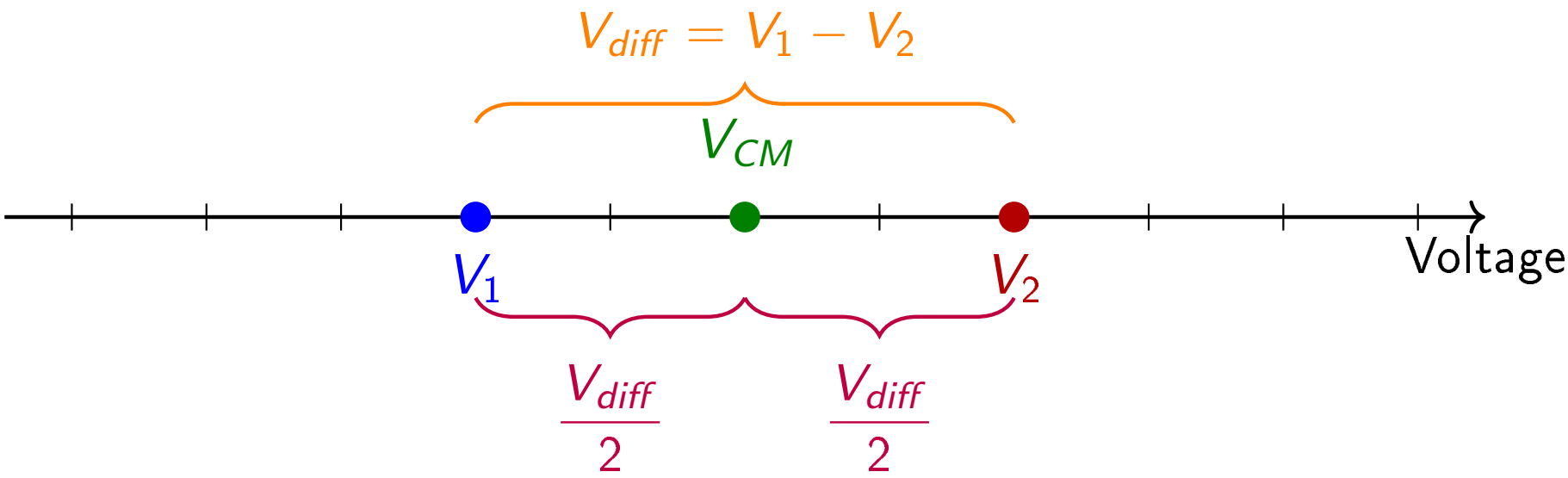
(the average — the midpoint)

Differential voltage:

$$V_{diff} = V_1 - V_2$$

(the difference — the spread)

Visualizing V_{CM} and V_{diff} on the Number Line



V_{CM} sits at the **midpoint** between V_1 and V_2. Each voltage is $V_{diff}/2$ away:

$$\boxed{V_1 = V_{CM} + \frac{V_{diff}}{2}} \qquad \boxed{V_2 = V_{CM} - \frac{V_{diff}}{2}}$$

Check: $V_1 + V_2 = 2\,V_{CM}$ ✓ $V_1 - V_2 = V_{diff}$ ✓

Why Decompose This Way?

Any pair (V_1, V_2) can be **uniquely** written as (V_{CM}, V_{diff})

The differential pair circuit responds **differently** to each:

- **Common-mode** (V_{CM}): shifts both inputs together — ideally **no effect** on V_{OUT}
- **Differential** (V_{diff}): pushes inputs apart — produces the **output signal**

This lets us analyze the circuit's response to each component **separately**

Key idea: The differential pair *amplifies the difference* V_{diff} and *rejects the common part* V_{CM}.

This is why it is called a **differential** amplifier.

Numerical Example

Suppose $V_1 = 3.2$ V and $V_2 = 2.8$ V.

Common-mode:

$$V_{CM} = \frac{3.2 + 2.8}{2} = 3.0 \text{ V}$$

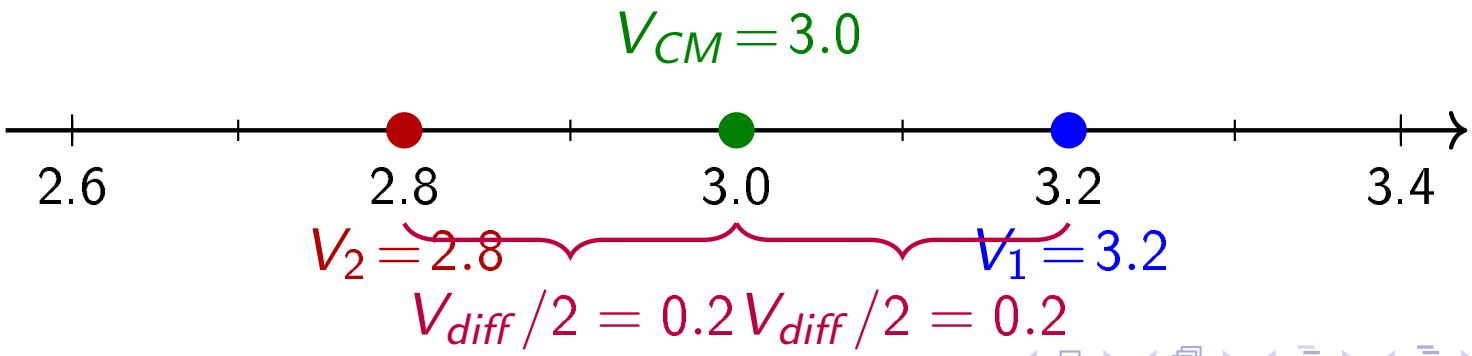
Differential:

$$V_{diff} = 3.2 - 2.8 = 0.4 \text{ V}$$

Reconstruct:

$$V_1 = 3.0 + \frac{0.4}{2} = 3.2 \text{ V} \checkmark$$

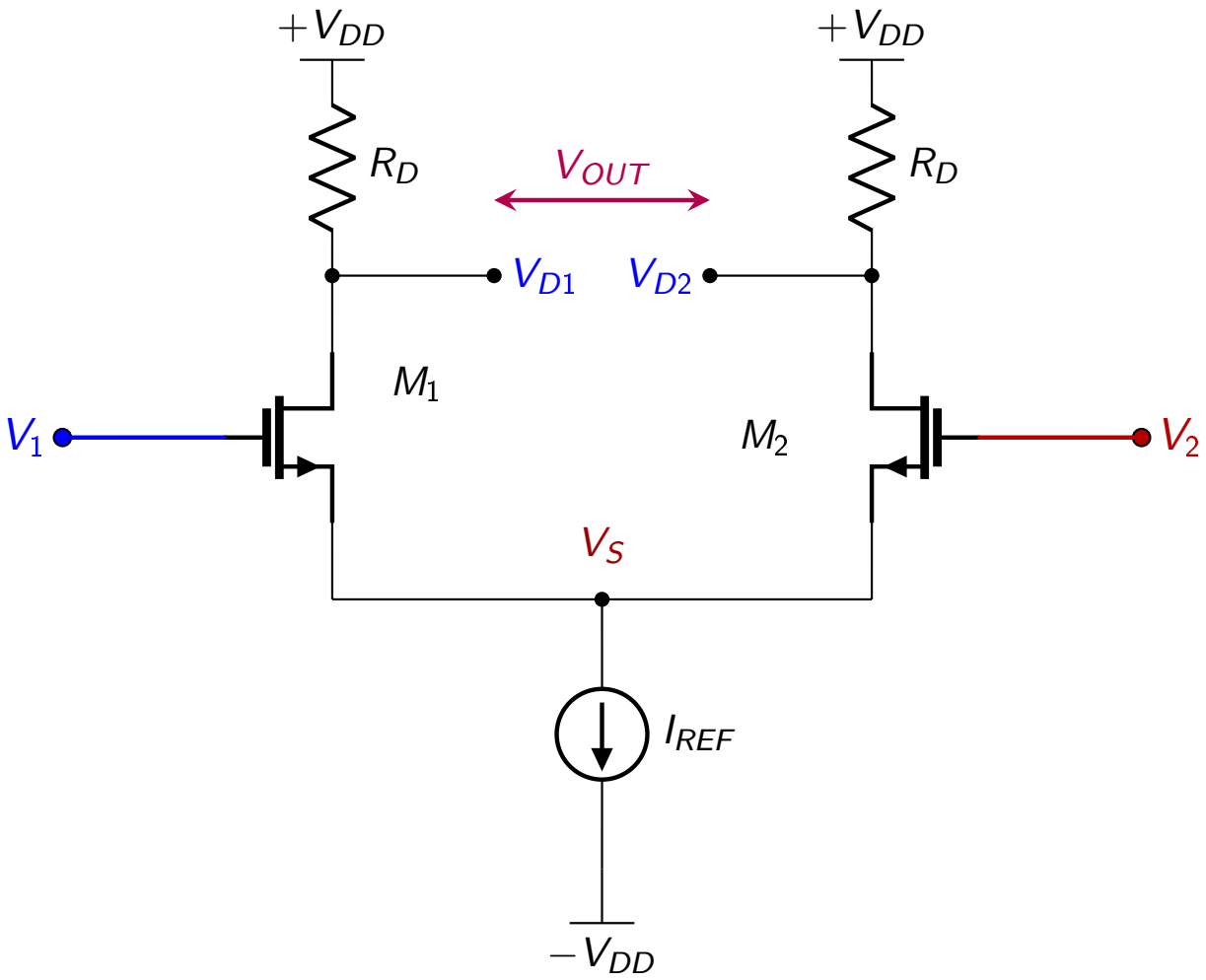
$$V_2 = 3.0 - \frac{0.4}{2} = 2.8 \text{ V} \checkmark$$



Differential Pair

with Two Different Inputs

Differential Pair with V_1 and V_2

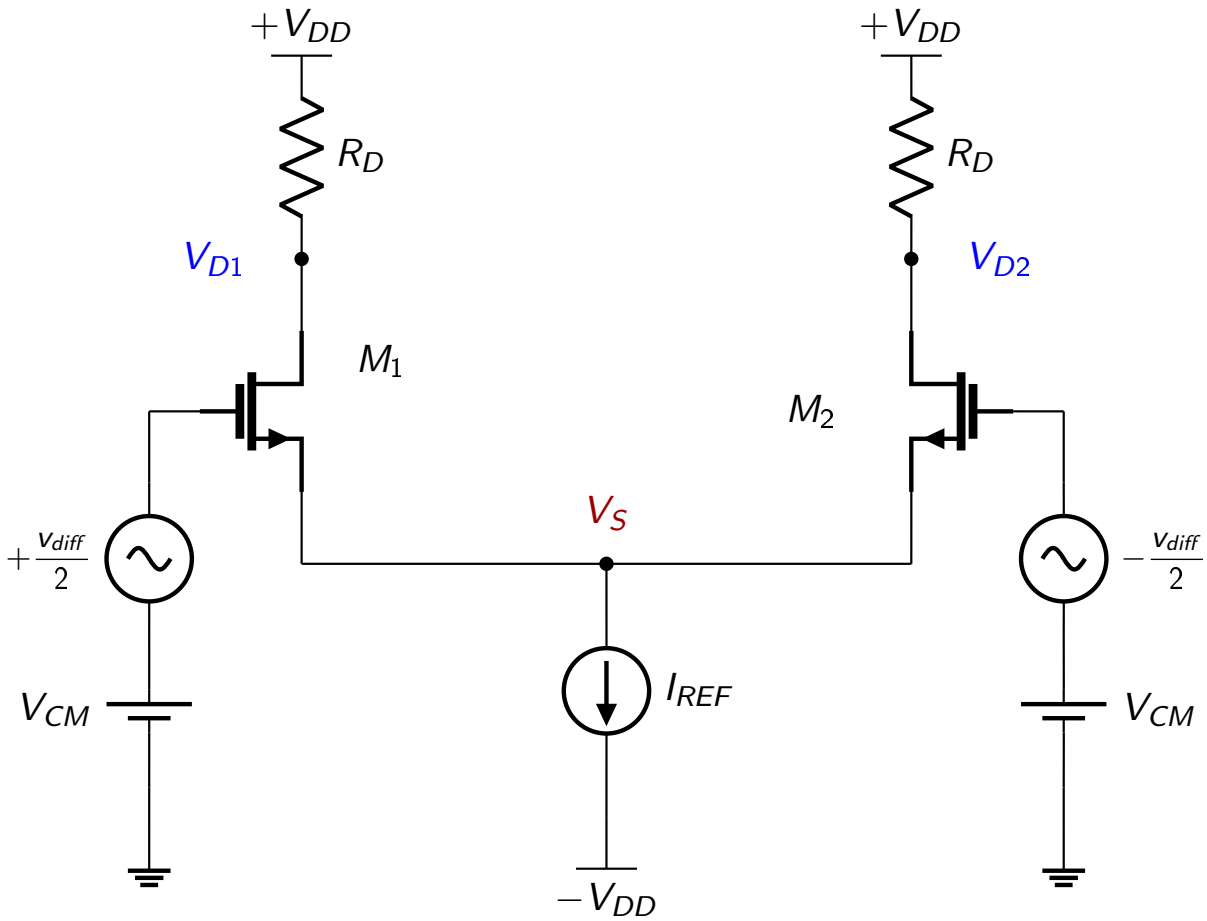


Now $V_1 \neq V_2$ — the gates are driven by **different** voltages.
How does the circuit respond?

Replace V_1, V_2 with V_{CM} and V_{diff}

Using our decomposition:

$$V_1 = V_{CM} + \frac{V_{diff}}{2}, \qquad V_2 = V_{CM} - \frac{V_{diff}}{2}$$



The Common-Mode Component: V_{CM}

V_{CM} sets the **operating point** (bias) of the differential pair

With no signal applied ($v_{diff} = 0$), both gates sit at V_{CM}

This is identical to Lecture 18 with $V_{BIAS} = V_{CM}$

The current splits equally: $I_{D1} = I_{D2} = I_{REF}/2$

The source voltage is:

$$V_S = V_{CM} - V_{GS}$$

where $V_{GS} = V_{TN} + V_{OV}$ is set by $I_{REF}/2$ flowing through each transistor

Since the current splits equally: $V_{OUT} = V_{D1} - V_{D2} = 0$ (as we saw in Lecture 18)

V_{CM} is a **large** voltage (on the order of the supply) — it determines the bias currents and node voltages

Because V_{CM} is large, we analyze its effect using the **large-signal model** of the MOSFETs (the I–V equations from Lecture 18).

The Differential Component: $\pm v_{diff}/2$

v_{diff} is the **signal** that the differential pair amplifies

It is **small** compared to V_{CM} — a small perturbation around the operating point

Applied with **opposite signs** to the two gates:

$$\underbrace{V_1 = V_{CM} + \frac{v_{diff}}{2}}_{\text{Gate 1}} \qquad \underbrace{V_2 = V_{CM} - \frac{v_{diff}}{2}}_{\text{Gate 2}}$$

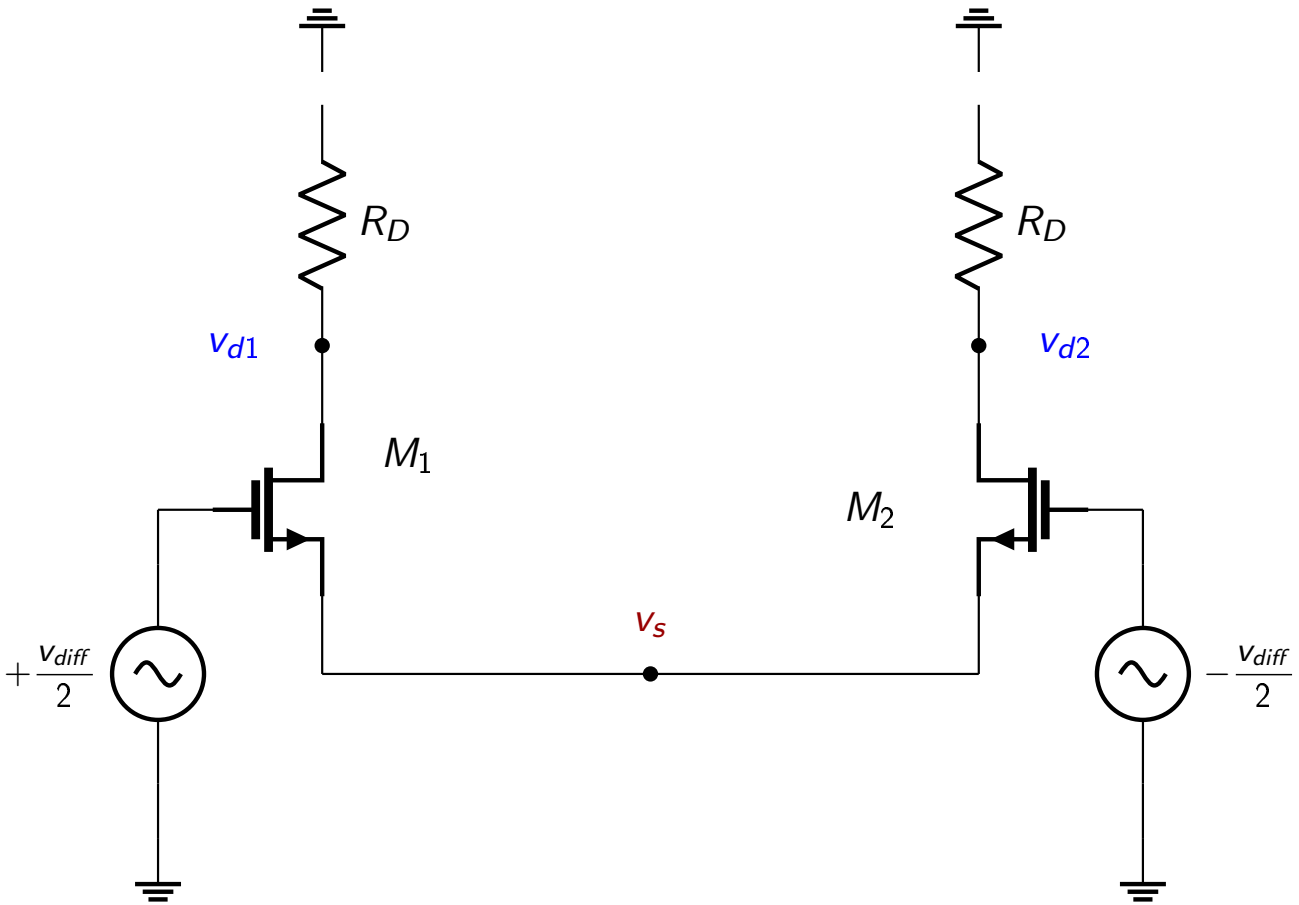
This pushes M_1 and M_2 in **opposite** directions

When $v_{diff} > 0$: V_{GS1} increases, V_{GS2} decreases

I_{D1} increases, I_{D2} decreases (but $I_{D1} + I_{D2} = I_{REF}$)

Because v_{diff} is small, we analyze its effect using the **small-signal model** of the MOSFETs (g_m, r_o) — linearized around the operating point set by V_{CM}.

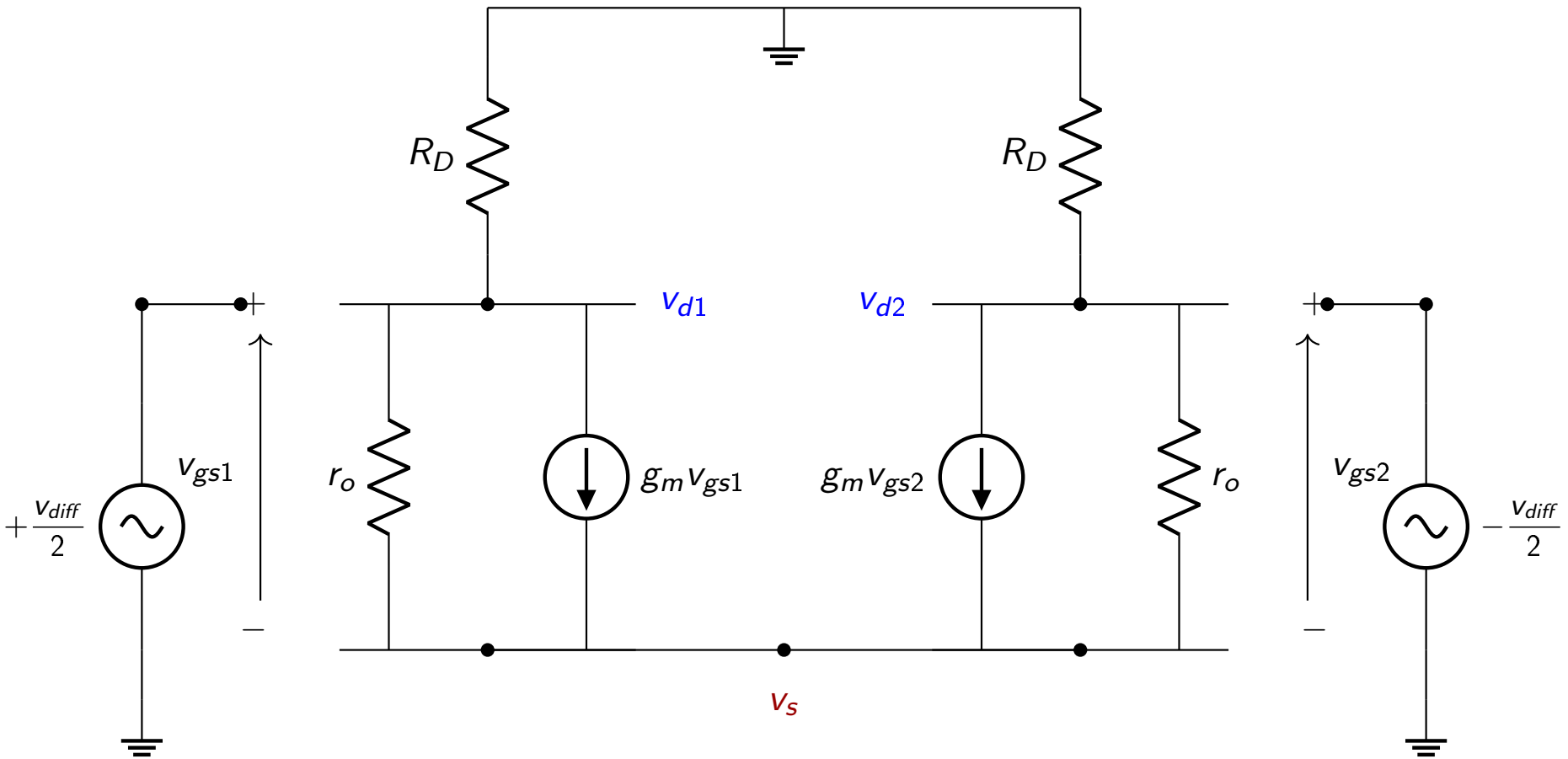
Small-Signal Circuit



DC supplies $\rightarrow$ ground, DC current source $\rightarrow$ open circuit, V_{CM} removed.

Only the small-signal sources $\pm v_{diff}/2$ remain.

Small-Signal Model



Each MOSFET replaced by its small-signal model: $g_m v_{gs}$ current source in parallel with r_o.

Matched Parameters

Since both transistors are biased by V_{CM} with equal currents $I_{D1} = I_{D2} = I_{REF}/2$, their small-signal parameters are **identical**:

Transconductance:

$$g_{m1} = g_{m2} \equiv g_m$$

$$g_m = \frac{2\,I_D}{V_{OV}} = \sqrt{2\,k_n' \frac{W}{L} I_D}$$

where $I_D = I_{REF}/2$

Output resistance:

$$r_{o1} = r_{o2} \equiv r_o$$

$$r_o = \frac{1}{\lambda\,I_D} = \frac{V_A}{I_D}$$

where $I_D = I_{REF}/2$

Both g_m and r_o depend only on $I_D = I_{REF}/2$, which is set by V_{CM}

The small-signal parameters are **not** functions of v_{diff} — they are constants determined at the operating point

Because the circuit is symmetric, we can write g_m and r_o without subscripts.

KCL at the Source Node v_s

Apply KCL at the shared source node (ignoring r_o for now). The currents flowing **into** v_s from M_1 and M_2:

$$g_m v_{gs1} + g_m v_{gs2} = 0$$

Substituting $v_{gs1} = \frac{v_{diff}}{2} - v_s$ and $v_{gs2} = -\frac{v_{diff}}{2} - v_s$:

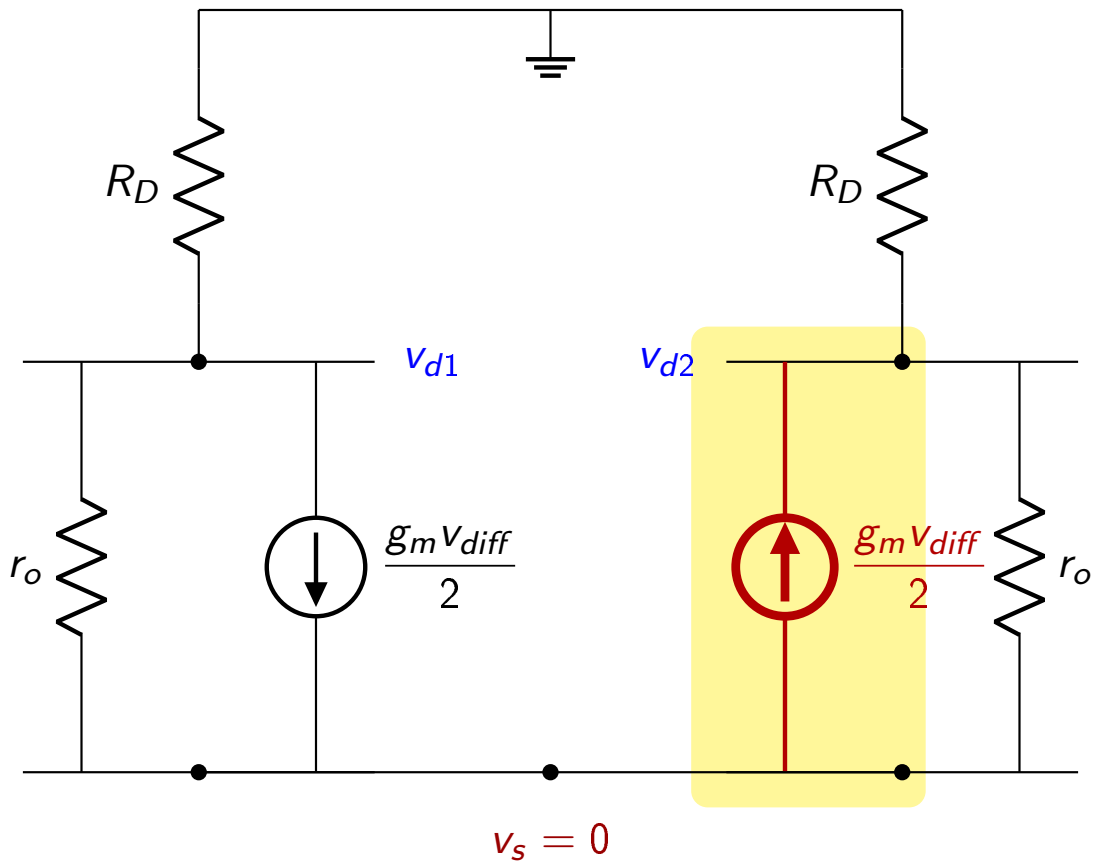
$$g_m\left(\frac{v_{diff}}{2} - v_s\right) + g_m\left(-\frac{v_{diff}}{2} - v_s\right) = 0$$

$$\cancel{g_m \frac{v_{diff}}{2}} - g_m v_s - \cancel{g_m \frac{v_{diff}}{2}} - g_m v_s = 0 \quad \Longrightarrow \quad \boxed{v_s = 0}$$

The source voltage is **always zero** regardless of v_{diff}.

When a node's voltage is zero no matter what signal is applied, we call it a **virtual ground**.

Substituting $v_s = 0$ into the Current Sources



$$g_m v_{gs2} = -\frac{g_m v_{diff}}{2} \text{ pointing } \textbf{down} = +\frac{g_m v_{diff}}{2} \text{ pointing } \textbf{up}$$

Both sources now push current in the **same direction** through the circuit.

Virtual Ground $\neq$ Actual Ground

$v_s = 0$ means the source node is at **zero voltage** — but it is **not connected to ground**

It is its own node and must satisfy **KCL independently**

Current that enters v_s through one r_o **cannot magically appear** at the ground on top of R_D

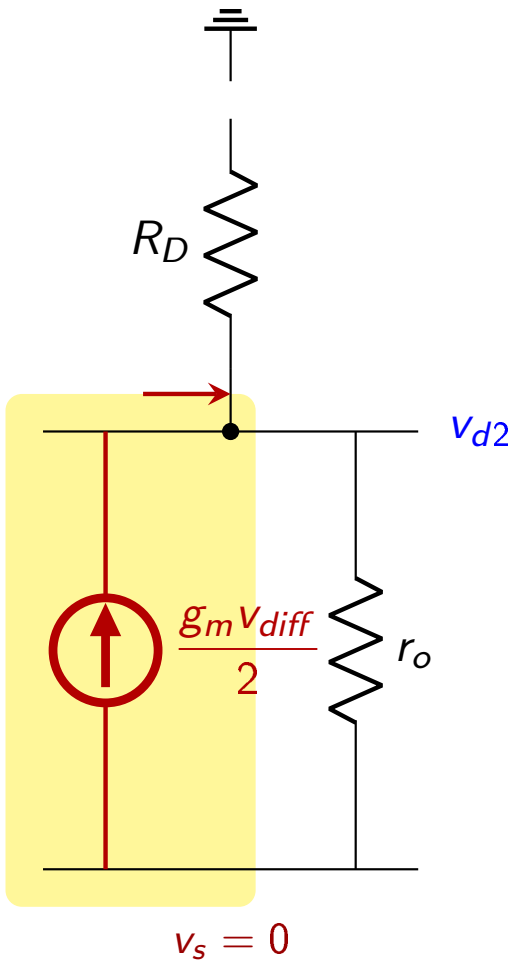
Instead, every electron that flows into v_s through r_{o1} is matched by an electron flowing **out of** v_s through r_{o2}

The two r_o currents cancel **at the source node** — they circulate between the two halves, not through ground

Actual ground: can sink or source unlimited current.

Virtual ground: voltage is zero, but current is **not** absorbed — it must go somewhere else in the circuit. KCL still applies.

Right Half: Current into the Drain of M_2



The current $\frac{g_m v_{diff}}{2}$ is injected **into** the drain node.

It must flow through R_D or r_o (in parallel):

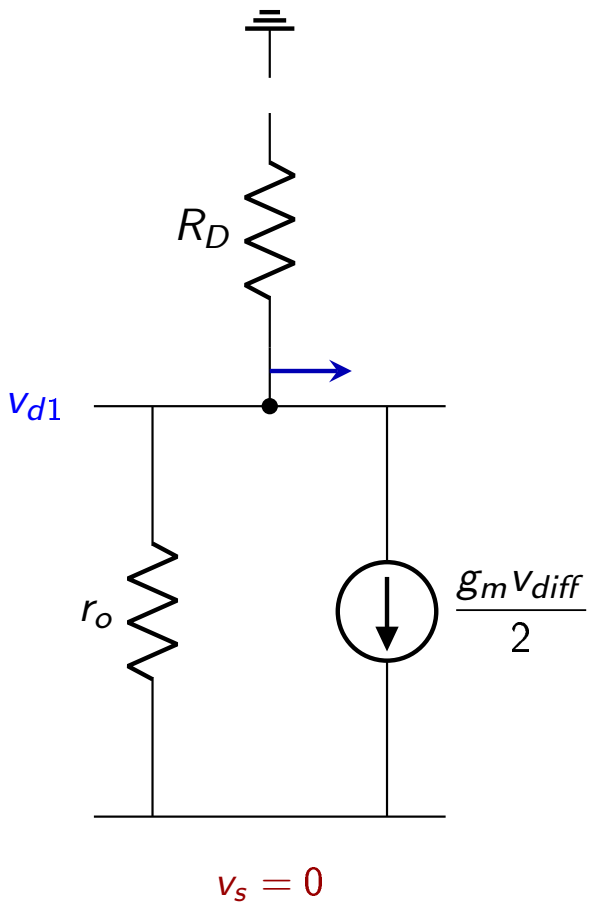
Since $r_o \gg R_D$:

$$R_D \| r_o \approx R_D$$

Nearly all current flows through R_D:

$$\boxed{v_{d2} = +\frac{g_m v_{diff}}{2} R_D}$$

Left Half: Current out of the Drain of M_1



The current $\frac{g_m v_{diff}}{2}$ is pulled **out of** the drain node (opposite direction).

Again $r_o \gg R_D$, so current flows through R_D:

$$\boxed{v_{d1} = -\frac{g_m v_{diff}}{2} R_D}$$

The **output voltage**:

$$\begin{aligned} v_{out} &= v_{d1} - v_{d2} \\ &= -\frac{g_m v_{diff}}{2} R_D - \frac{g_m v_{diff}}{2} R_D \end{aligned}$$

$$\boxed{v_{out} = -g_m R_D v_{diff}}$$

Differential Gain

The **differential voltage gain** of the differential pair:

If we define $v_{out} = v_{d1} - v_{d2}$:

$$\boxed{A_{diff} = \frac{v_{out}}{v_{diff}} = -g_m R_D}$$

If instead $v_{out} = v_{d2} - v_{d1}$:

$$A_{diff} = \frac{v_{out}}{v_{diff}} = +g_m R_D$$

Whether the gain is inverting or non-inverting depends on **which output you call positive**

The gain magnitude $|A_{diff}| = g_m R_D$ depends on bias current and R_D

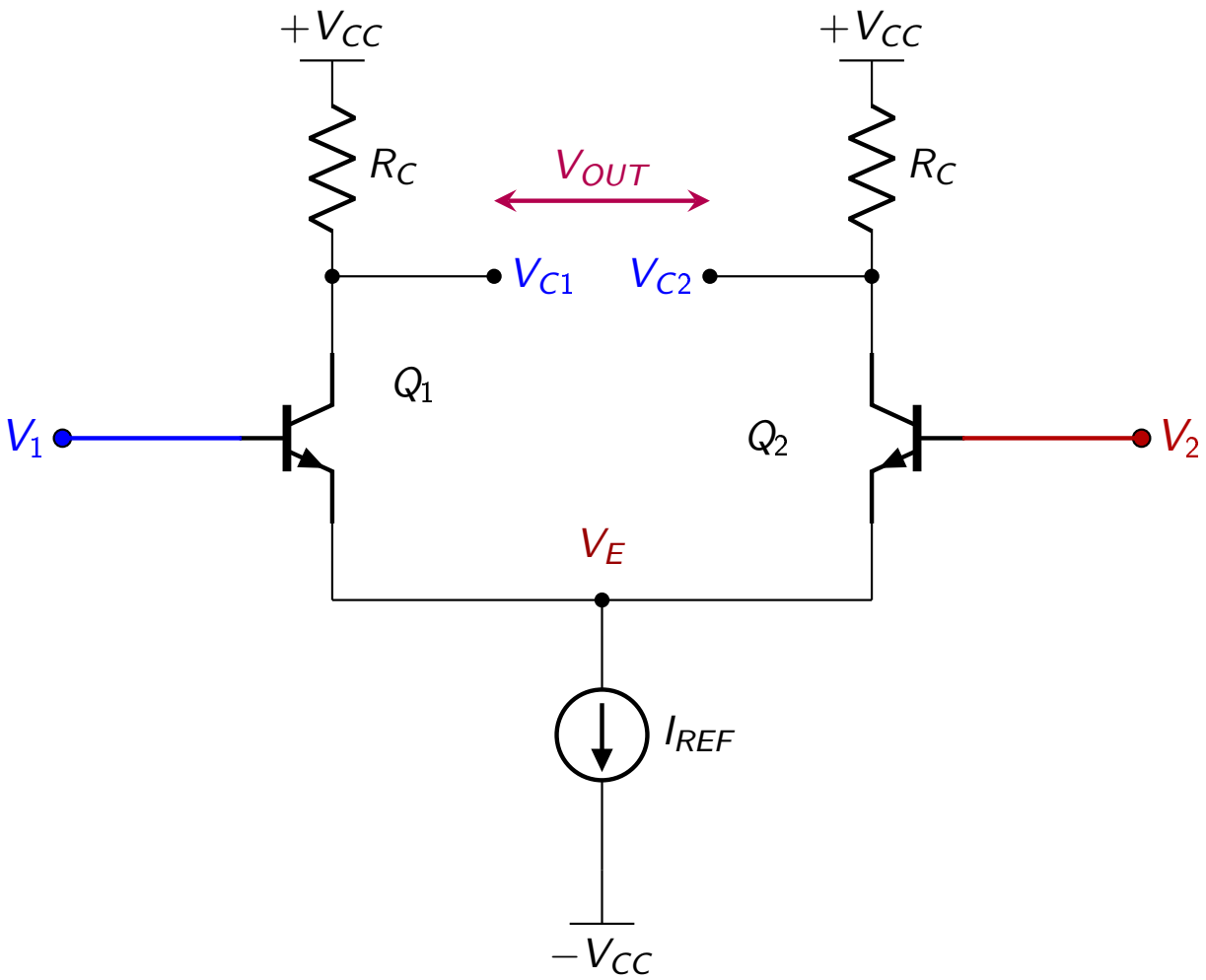
r_o does not appear because $r_o \gg R_D$

Think of V_1 as V^+ and V_2 as V^-, just like an **op amp**.
The differential pair *is* the input stage of an op amp!

BJT Differential Pair

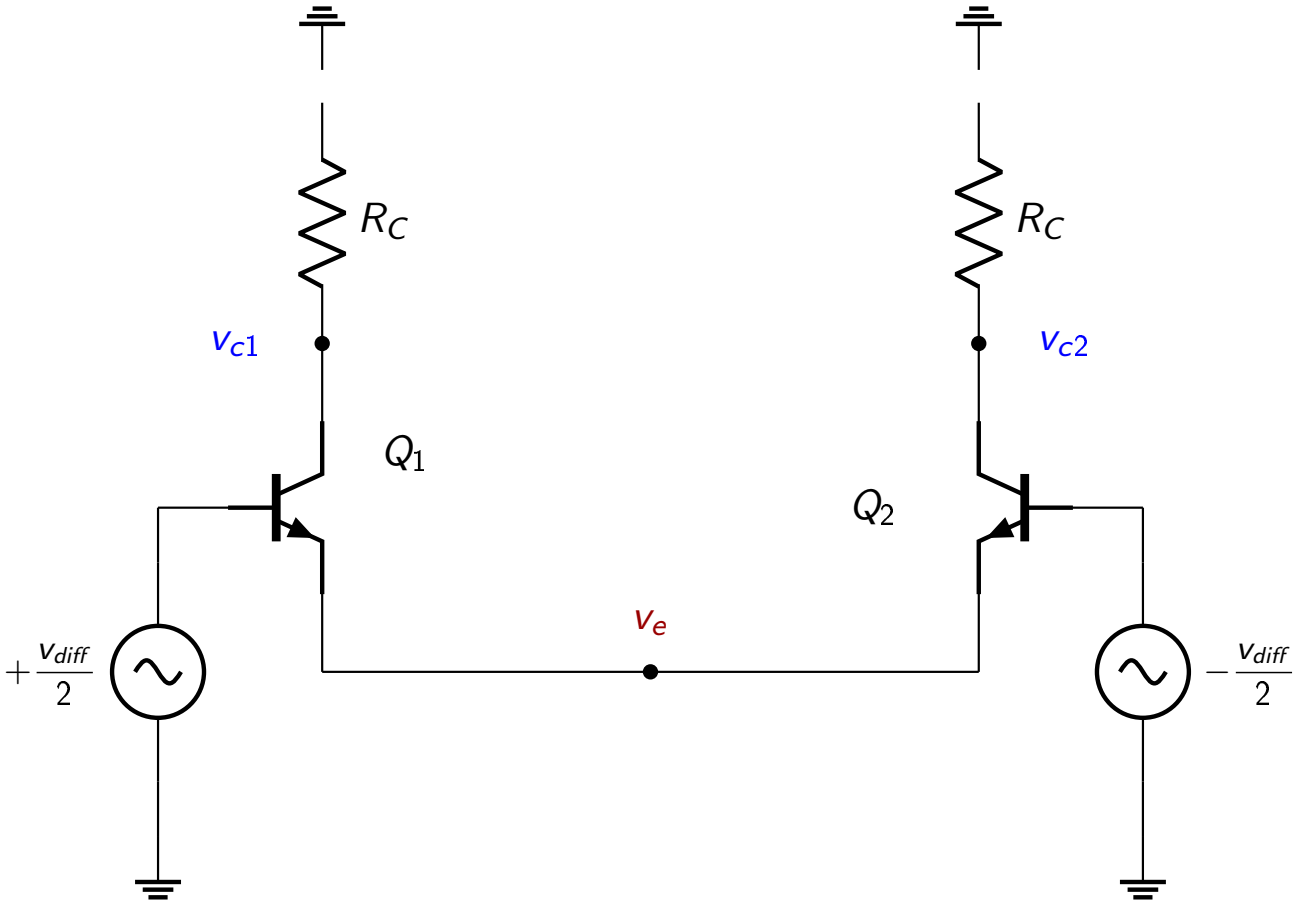
Same Analysis, Different Device

BJT Differential Pair with V_1 and V_2



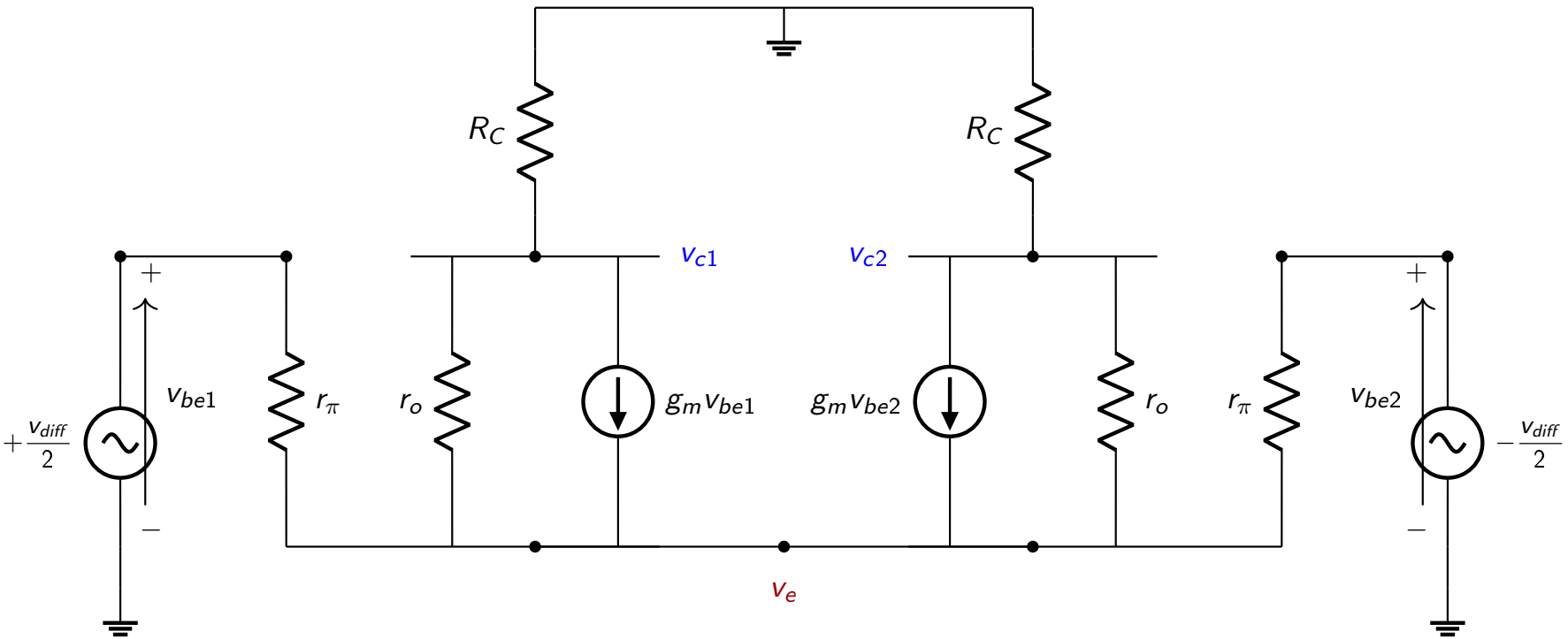
Same topology as the MOSFET pair: $V_1 \neq V_2$, Q_1 and Q_2 matched.

BJT Small-Signal Circuit



DC supplies $\rightarrow$ ground, DC current source $\rightarrow$ open circuit, V_{CM} removed.

BJT Small-Signal Model



BJT model adds r_π between base and emitter (finite input impedance).

BJT Matched Parameters

Since both transistors are biased by V_{CM} with equal currents $I_{C1} = I_{C2} = I_{REF}/2$:

Transconductance:

$$g_{m1} = g_{m2} \equiv g_m$$
$$g_m = \frac{I_C}{V_T}$$

Input resistance:

$$r_{\pi 1} = r_{\pi 2} \equiv r_\pi$$
$$r_\pi = \frac{\beta}{g_m}$$

Output resistance:

$$r_{o1} = r_{o2} \equiv r_o$$
$$r_o = \frac{V_A}{I_C}$$

where $I_C = I_{REF}/2$ and $V_T \approx 26$ mV at room temperature.

All parameters depend only on $I_C = I_{REF}/2$, set by V_{CM}

Key difference from MOSFET: BJT has finite r_π (MOSFET gate has $r_\pi \to \infty$)

Circuit symmetry $\Rightarrow$ we drop subscripts: g_m, r_π, r_o.

BJT: KCL at the Emitter Node v_e

By **symmetry**, the same argument as the MOSFET case applies.

Currents into v_e from Q_1: through $g_m v_{be1}$, r_{o1}, and $r_{\pi 1}$

Currents into v_e from Q_2: through $g_m v_{be2}$, r_{o2}, and $r_{\pi 2}$

Since the circuit is symmetric and the inputs are antisymmetric ($+v_{diff}/2$ and $-v_{diff}/2$):

- Every current flowing into v_e from Q_1 is matched by an equal current flowing **out** through Q_2
- This includes currents through g_m, r_o, **and** r_π
- The base currents $i_{b1} = v_{be1}/r_\pi$ and $i_{b2} = v_{be2}/r_\pi$ are **equal and opposite** since $v_{be1} = -v_{be2}$ — they cancel at v_e

The base currents through r_π cancel by symmetry — the virtual ground holds even with finite input impedance.

BJT: Virtual Ground at v_e

All currents cancel at the emitter node, therefore:

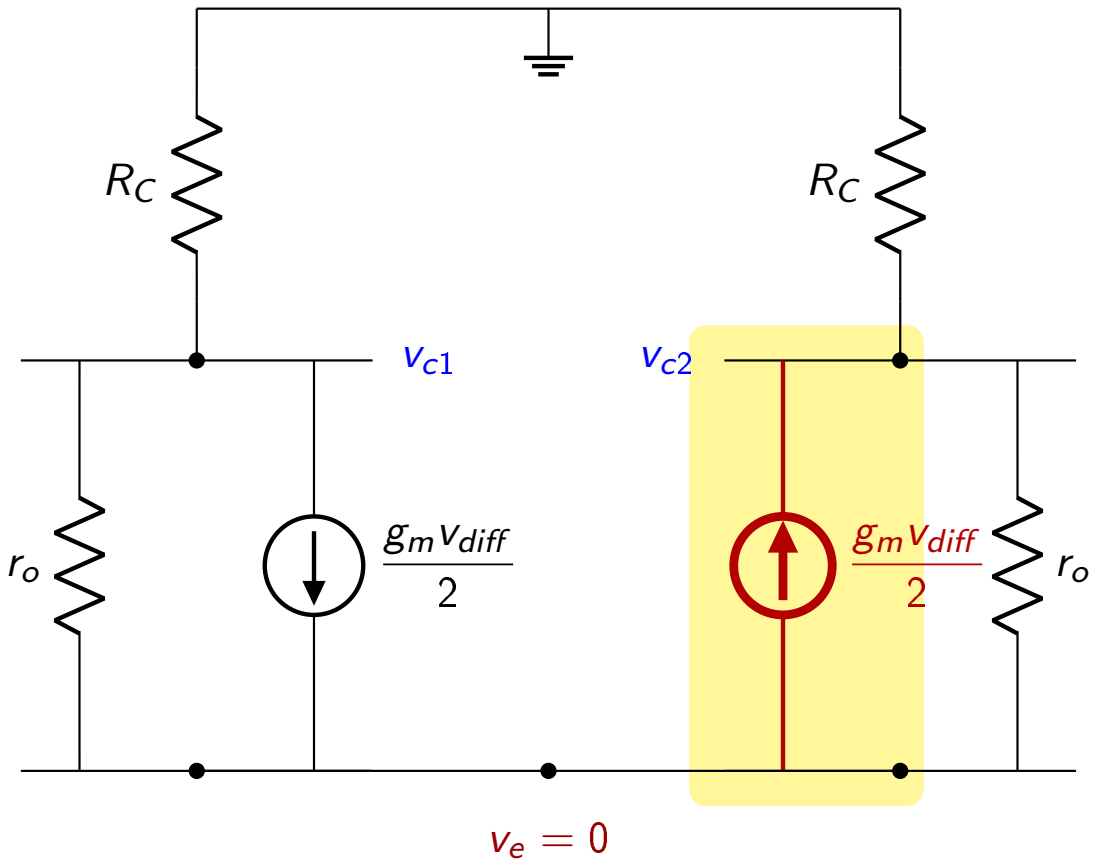
$$\boxed{v_e = 0} \qquad \text{(virtual ground, same as MOSFET)}$$

Since $v_e = 0$:

$$v_{be1} = v_1 - v_e = +\frac{v_{diff}}{2}, \qquad v_{be2} = v_2 - v_e = -\frac{v_{diff}}{2}$$

With $v_e = 0$, each v_{be} is fully determined by the input signal.
We can now substitute directly into the current sources.

BJT: Substituting $v_e = 0$ into the Current Sources



Same result as MOSFET: both sources push $\frac{g_m v_{diff}}{2}$ in the **same direction**.

BJT: Half-Circuit Analysis

Right half (Q_2): Current injected **into** collector.

Since $r_o \gg R_C$:

$$\boxed{v_{c2} = +\frac{g_m\, v_{diff}}{2} R_C}$$

Left half (Q_1): Current pulled **out of** collector.

$$\boxed{v_{c1} = -\frac{g_m\, v_{diff}}{2} R_C}$$

Output voltage:

$$\begin{aligned} v_{out} &= v_{c2} - v_{c1} \\ &= +\frac{g_m v_{diff}}{2} R_C + \frac{g_m v_{diff}}{2} R_C \end{aligned}$$

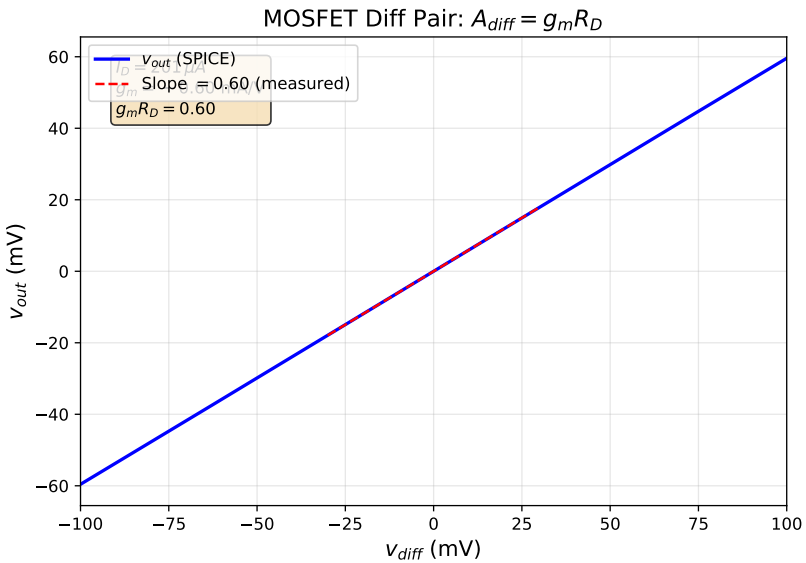
$$\boxed{v_{out} = +g_m\, R_C\, v_{diff}}$$

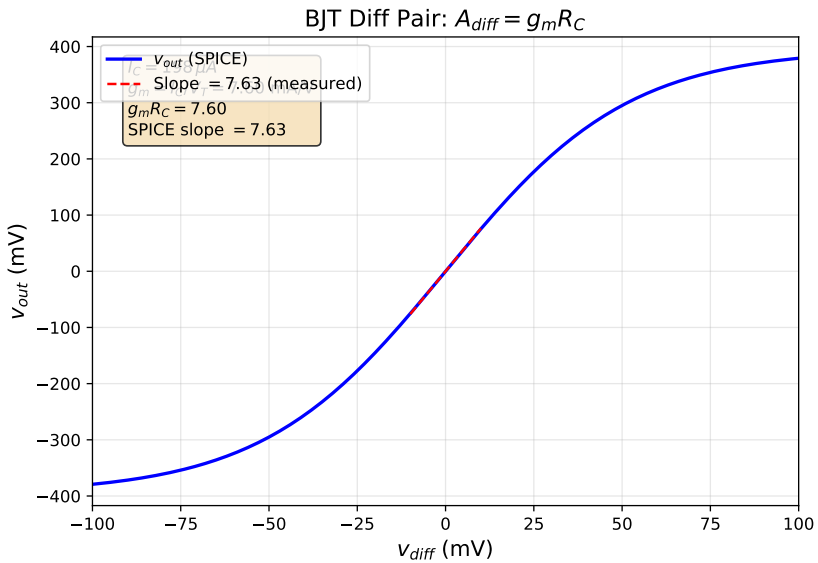
Differential gain:

$$\boxed{A_{diff} = \frac{v_{out}}{v_{diff}} = +g_m\, R_C}$$

Identical form to the MOSFET result! Just replace $R_D \to R_C$.
The only difference: BJT has $g_m = I_C/V_T$ vs. MOSFET $g_m = 2I_D/V_{OV}$.

SPICE Verification of Differential Gain





SPICE confirms $A_{diff} = g_m R_D$ (MOSFET) and $A_{diff} = g_m R_C$ (BJT). Linear region is narrow for BJT (± 10 mV) vs. MOSFET (± 50 mV) because BJT g_m is much larger.

Lecture 19 Summary

Any two voltages V_1, V_2 can be decomposed into:

Common-mode: $V_{CM} = (V_1 + V_2)/2$ (large, sets bias)
Differential: $v_{diff} = V_1 - V_2$ (small, is the signal)

V_{CM} is analyzed with the **large-signal model** (Lecture 18)

v_{diff} is analyzed with the **small-signal model**

By symmetry, the shared source/emitter node is a **virtual ground** ($v_s = 0$ or $v_e = 0$)

Virtual ground $\neq$ actual ground: KCL still applies, no current is absorbed

The circuit splits into two **half-circuits** at the virtual ground

Differential gain:

MOSFET: $A_{diff} = g_m R_D$ BJT: $A_{diff} = g_m R_C$

Sign of gain depends on definition of v_{out} (V^+ vs V^-, like an op amp)

BJT has higher $g_m = I_C/V_T$ but narrower linear range than MOSFET

Next: What happens when the circuit is *not* perfectly symmetric? Common-mode rejection ratio (CMRR).