EE461g: Introduction to Electronic Circuits

Lecture 20

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Outline

Active Load

Differential Pair

Lecture 19 Recap

In Lecture 19, we found the differential gain with resistor loads:

$$A_{diff} = g_m R_D$$

To increase gain, we need larger R_D or larger g_m

But larger R_D means larger voltage drop $I_D \cdot R_D$

- Reduces output voltage swing
- Requires higher supply voltage
- Large resistors are expensive in IC design

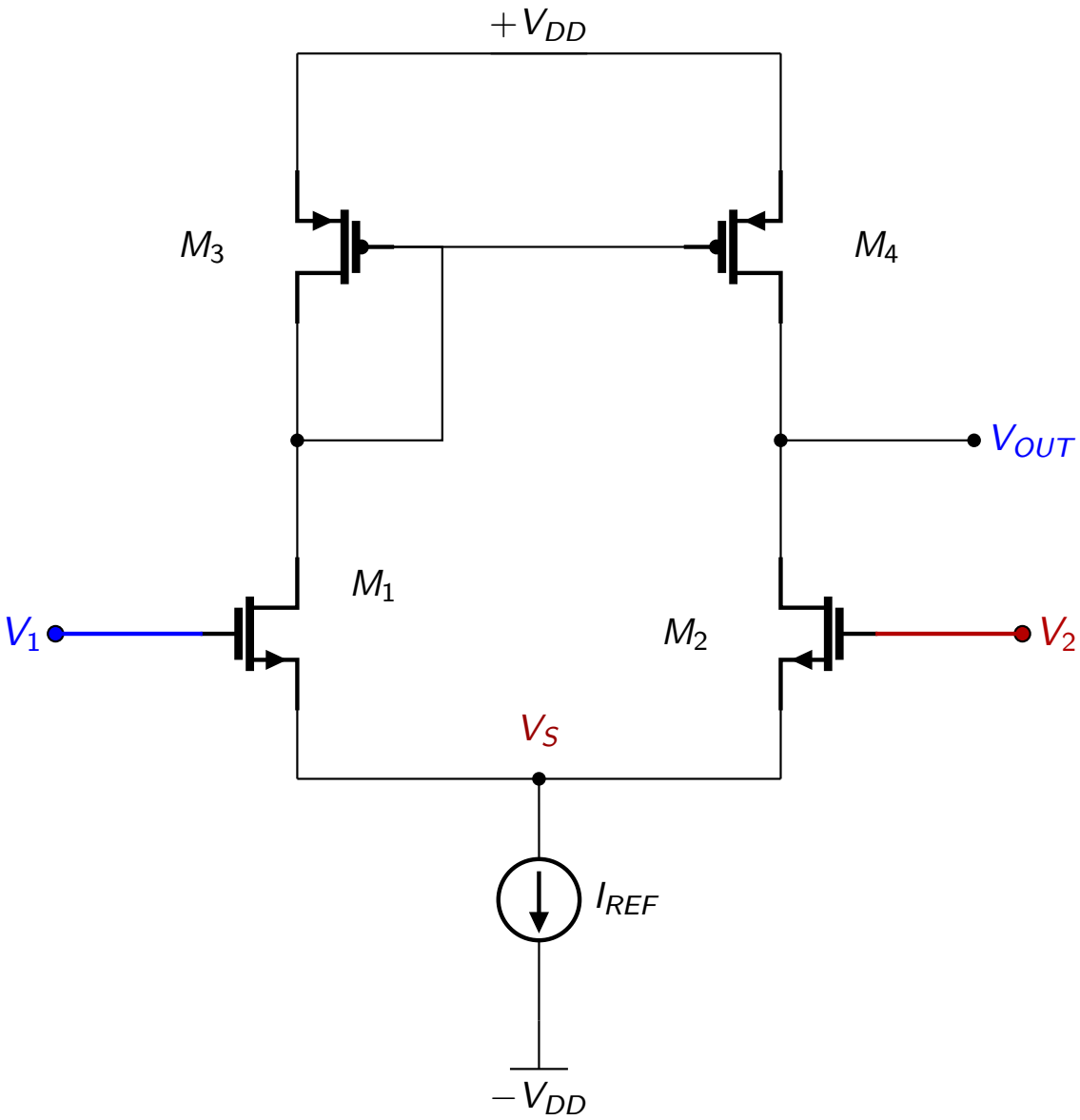
Solution: Replace R_D with a **current mirror** (active load)

A current source has very high output resistance (r_o) but only a small DC voltage drop (V_{OV}). This gives us high gain **and** large output swing.

MOSFET Diff Pair

with PMOS Current Mirror Load

The Circuit



How the Active Load Works

M_3 is **diode-connected** (gate tied to drain) — it acts as a "resistor" that sets the current

M_4 **mirrors** the current through M_3: if M_3 and M_4 are matched, $I_{D4} = I_{D3}$

At the bias point ($v_{diff} = 0$):

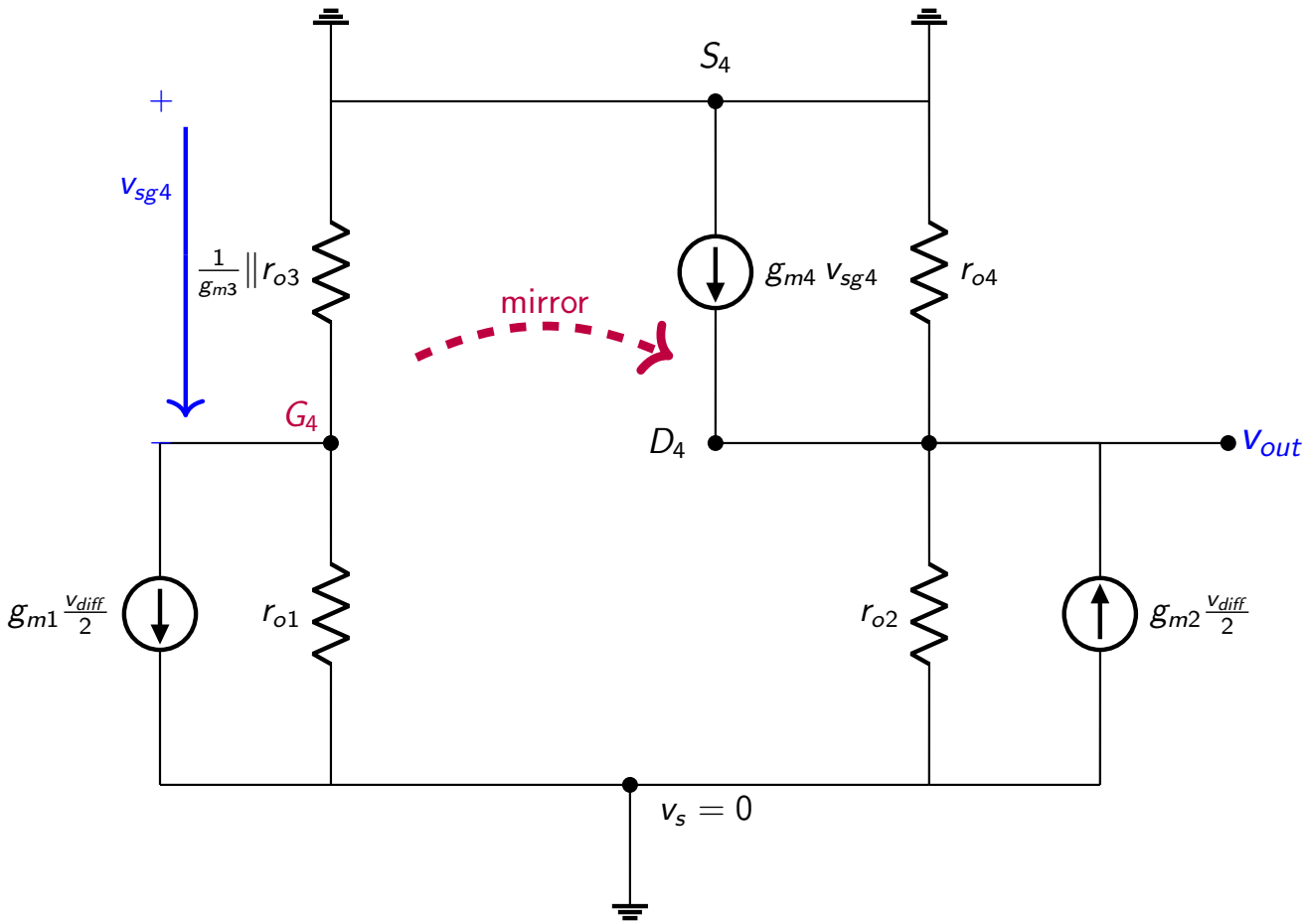
$I_{D1} = I_{D2} = I_{REF}/2$
M_3 forces $I_{D3} = I_{D1} = I_{REF}/2$
M_4 mirrors this: $I_{D4} = I_{REF}/2 = I_{D2}$ ✓

The output is taken **single-ended** from the drain of M_2 (= drain of M_4)

Key difference from Lecture 19: only **one** output node, not $V_{D1} - V_{D2}$

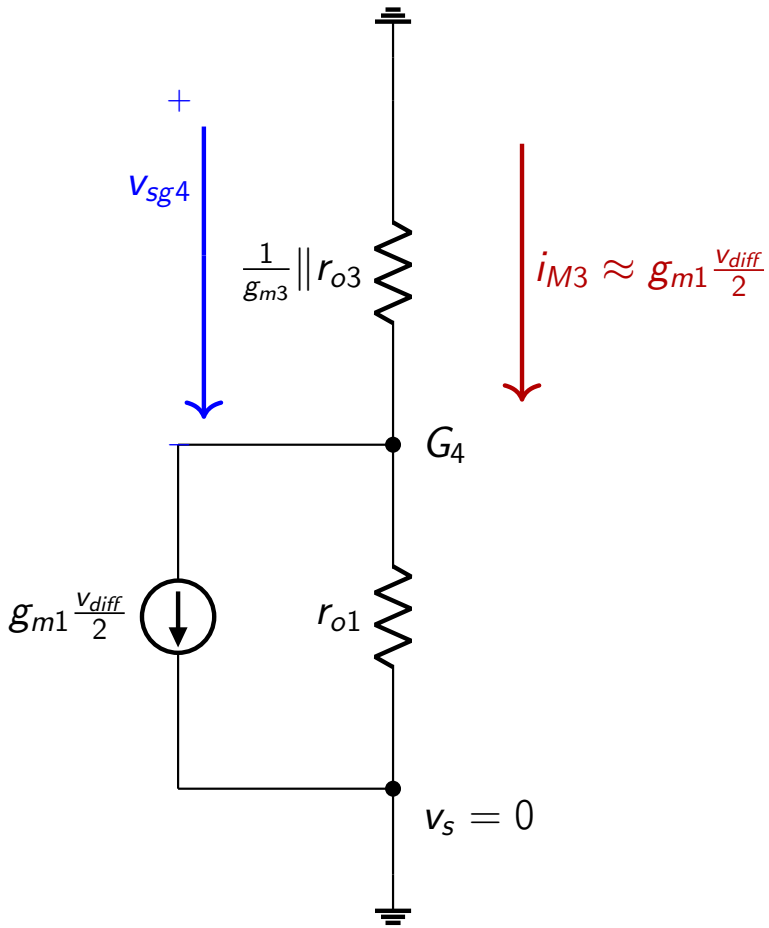
The PMOS mirror converts the differential pair's **two** output currents into a **single** output voltage at the M_2/M_4 drain node.

Small-Signal Equivalent Circuit



Left: M_1 drives current into diode-connected M_3 ($\approx 1/g_{m3}$). Right: M_4 mirrors that current; M_2 steers its own. Both act on v_{out}.

Left Half: M_1 and M_3



$$v_{sg4} = \frac{v_{diff}}{2}$$

Analyzing the Left Half

Step 1: Simplify the M_3 resistance.
Since $r_{o3} \gg \frac{1}{g_{m3}}$:

$$\frac{1}{g_{m3}} \| r_{o3} = \frac{r_{o3}}{1 + g_{m3}\, r_{o3}} \approx \frac{1}{g_{m3}}$$

Step 2: Nearly all of M_1's signal current flows through $\frac{1}{g_{m3}}$.
The current divider between r_{o1} and $\frac{1}{g_{m3}}$:

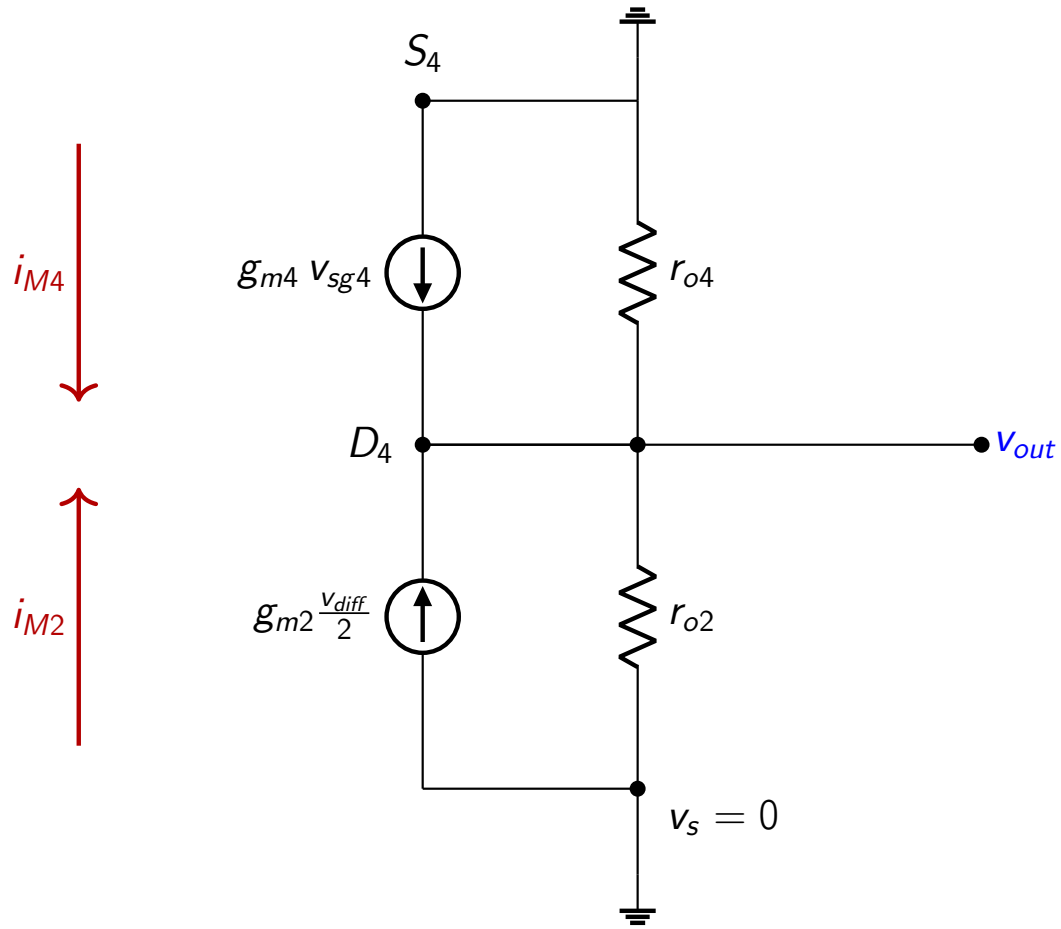
$$i_{M3} = g_{m1} \frac{v_{diff}}{2} \cdot \frac{r_{o1}}{r_{o1} + \frac{1}{g_{m3}}} \approx g_{m1} \frac{v_{diff}}{2} \quad \left(\text{since } r_{o1} \gg \frac{1}{g_{m3}}\right)$$

Step 3: Find v_{sg4} across the $\frac{1}{g_{m3}}$ resistor.

$$v_{sg4} = i_{M3} \cdot \frac{1}{g_{m3}} = \cancel{g_{m1}} \frac{v_{diff}}{2} \cdot \frac{1}{\cancel{g_{m3}}} = \frac{v_{diff}}{2} \quad (\text{matched: } g_{m1} = g_{m3})$$

$$v_{sg4} = \frac{v_{diff}}{2}$$

Right Half: M_2 and M_4



$$i_{M4} = g_{m4}\, v_{sg4} = g_{m4}\frac{v_{diff}}{2} \qquad i_{M2} = g_{m2}\frac{v_{diff}}{2}$$

General Gain Derivation

No assumptions about g_m matching between NMOS and PMOS.

From the left half: $v_{sg4} = g_{m1}\dfrac{v_{diff}}{2}\cdot\dfrac{1}{g_{m3}}$ Mirror current:

$$i_{M4} = \frac{g_{m4}}{g_{m3}}\cdot g_{m1}\frac{v_{diff}}{2}$$

M_2 current change: $\Delta i_{M2} = g_{m2}\dfrac{v_{diff}}{2}$ Total current into output:

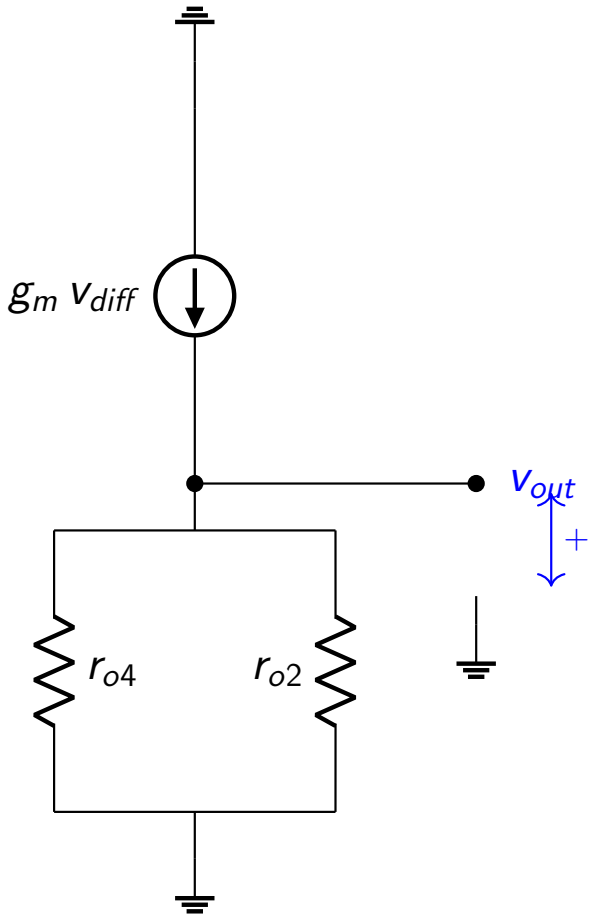
$$i_{out} = \frac{1}{2}\left(g_{m2} + \frac{g_{m4}}{g_{m3}}g_{m1}\right)v_{diff}$$

Since M_3, M_4 are matched PMOS: $g_{m4}/g_{m3} = 1$. Since M_1, M_2 are matched NMOS: $g_{m1} = g_{m2} = g_{m,n}$

$$\boxed{A_{diff} = g_{m,n}\left(r_{o2}\|r_{o4}\right)}$$

The gain depends on the **NMOS** g_m only. The PMOS g_m's cancel in the mirror.
r_{o2} (NMOS) and r_{o4} (PMOS) need not be equal.

Finding v_{out}



Total current into output node:

M_4 pushes $+g_m \frac{v_{diff}}{2}$ in (from mirror)

M_2 pushes $+g_m \frac{v_{diff}}{2}$ from shared source

$$i_{out} = g_m \frac{v_{diff}}{2} + g_m \frac{v_{diff}}{2} = g_m\, v_{diff}$$

This current flows through $r_{o2} \| r_{o4}$:

$$v_{out} = i_{out}(r_{o2} \| r_{o4}) = g_m\, v_{diff}\, (r_{o2} \| r_{o4})$$

$$\boxed{A_{diff} = g_m\, (r_{o2} \| r_{o4}) \approx \frac{g_m\, r_o}{2}}$$

Both halves contribute to the output. The gain is set by g_m and the parallel r_o's.

Input Impedance

The differential input impedance is seen looking into the gates of M_1 and M_2.

MOSFET gates draw **no DC current** ($I_G = 0$)

The small-signal gate current is also zero

Therefore:

$$\boxed{R_{in,diff} = \infty}$$

This is a major advantage of the MOSFET differential pair

The input does not load the previous stage

For BJT: $R_{in,diff} = 2\,r_\pi = 2\,\frac{\beta}{g_m}$ (finite, but still large)

Infinite input impedance means the diff pair can sense voltages without drawing current from the source.

Output Resistance at the Output Node

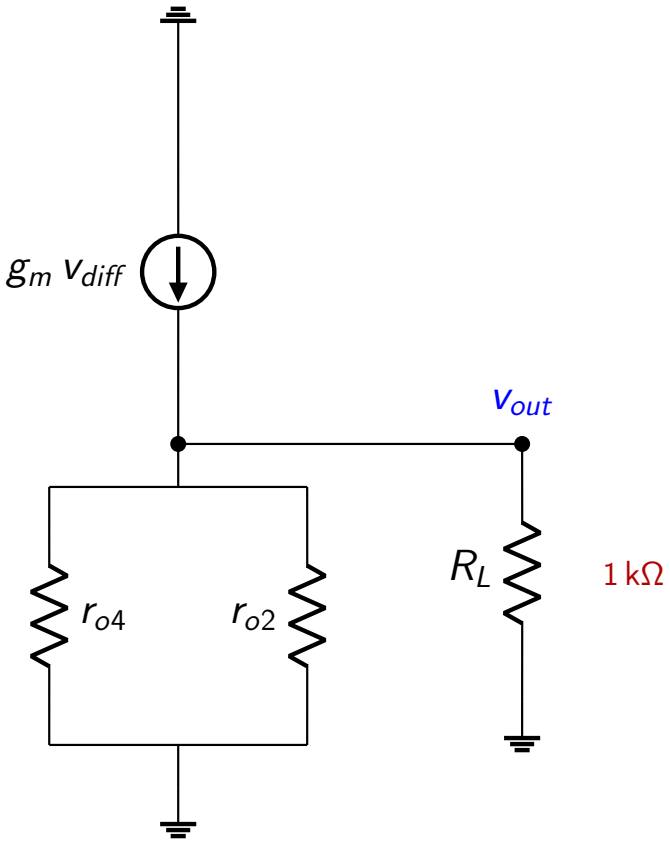
The output node sees two current sources looking in:

Looking down into M_2 (NMOS): output resistance r_{o2}

Looking up into M_4 (PMOS mirror): output resistance r_{o4}

These are in **parallel**: $R_{out} = r_{o2} \| r_{o4} \approx \frac{r_o}{2}$ (matched devices)

What Happens with a Load Resistor?



With a load R_L connected to the output:

The total resistance at the output becomes:

$$R_L \| r_{o2} \| r_{o4} \approx R_L \quad (\text{since } R_L \ll r_o)$$

Almost all of i_{out} flows through R_L, not r_o's:

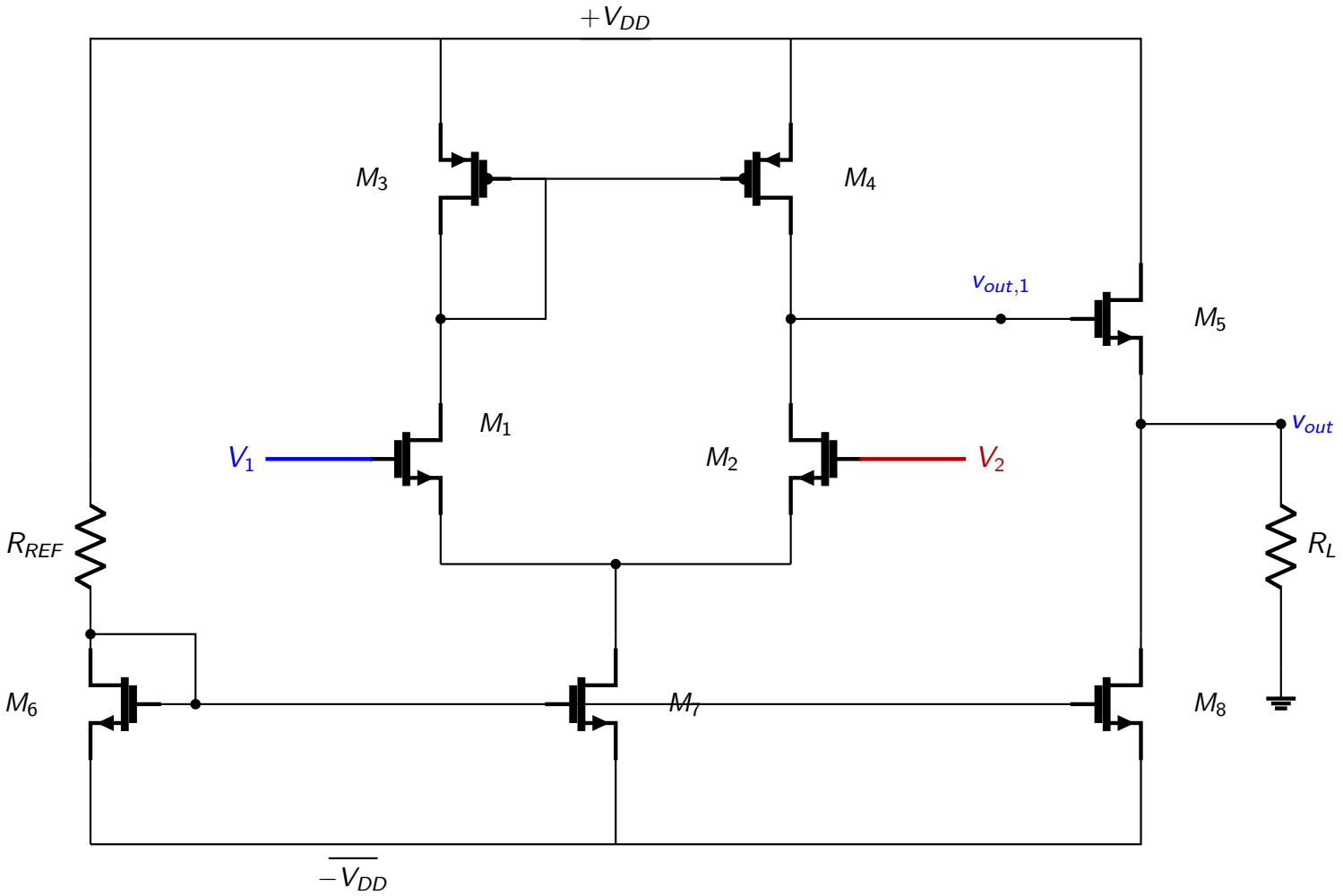
$$A_{diff} = g_m \left(R_L \| r_{o2} \| r_{o4}\right) \approx g_m R_L$$

Example: $g_m = 0.4$ mA/V, $R_L = 1$ kΩ:

$$A_{diff} \approx 0.4 \times 1 = 0.4 \quad \text{vs.} \quad 100 \text{ (no load)}$$

A small load resistor destroys the high gain! The active load's advantage ($r_o \gg R_D$) is lost when $R_L \ll r_o$. This is why op amps need **feedback**, not resistive loads.

Complete Circuit for SPICE Simulation



SPICE Simulation

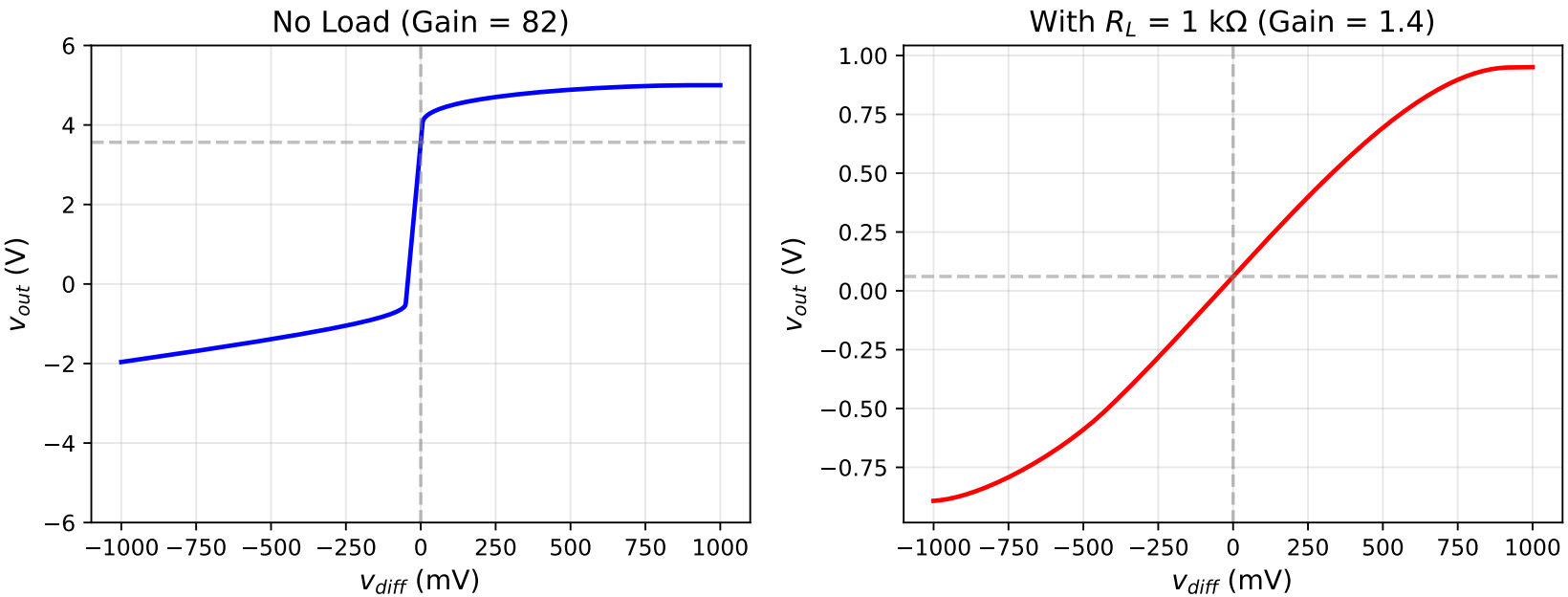
```
* Active-Load Diff Pair
VDD vdd 0 5
VSS vss 0 -5

* NMOS mirror tail (from Lec 17)
RREF vdd refnode 10k
M6 refnode refnode vss vss NMOS
+  W=10u L=1u
M7 tail refnode vss vss NMOS
+  W=10u L=1u

* Diff pair inputs
V1 gate1 0 0
V2 gate2 0 0

* NMOS diff pair
M1 drain1 gate1 tail tail NMOS
+  W=10u L=1u
M2 out gate2 tail tail NMOS
+  W=10u L=1u

* PMOS current mirror load
M3 drain1 drain1 vdd vdd PMOS
+  W=10u L=1u
M4 out drain1 vdd vdd PMOS
+  W=10u L=1u
```

SPICE confirms the theory:

	Formula	Thy	SPICE
No load	$g_{m,n}(r_{o2} \| r_{o4})$	83	**82**
$R_L = 1\text{k}$	$g_{m,n} R_L$	1.40	**1.39**
Buffered	$g_{m,n}(r_{o2} \| r_{o4}) \cdot \frac{g_5 R_L}{1+g_5 R_L}$	76	**76**

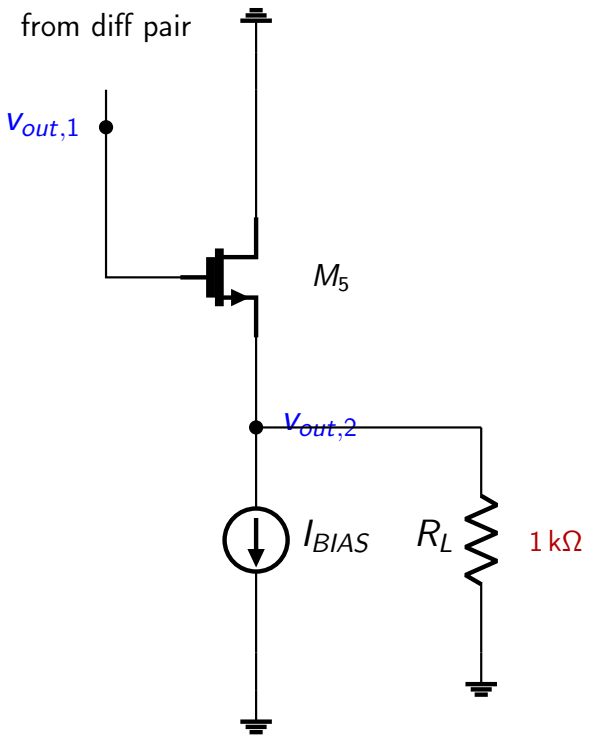
$g_{m,n} = 1.40$ mA/V, $r_o \approx 118$ kΩ, $g_{m5} = 12.0$ mA/V
$I_{REF} \approx 900\ \mu$A, M_5: $W/L = 100$, ± 5 V supplies, $R_{REF} = 10$ kΩ

SPICE: v_{out} vs. v_{diff}



Left: steep slope = high gain (82). Right: shallow slope = gain reduced by R_L (1.4).
The 1 kΩ load reduces the gain by a factor of ∼59×.

Solution: Buffer with a Source Follower



Common-drain (source follower):

Input Z: ∞ (MOSFET gate) — doesn't load diff pair

Output Z: $\approx 1/g_{m5}$ (low)

$I_{D5} = I_{BIAS} + V_{out}/R_L \approx$
$900\mu + 2490\mu = 3.4$ mA

$g_{m5} = 12.0$ mA/V (R_L boosts g_m!)

Buffer gain: $\dfrac{g_{m5}R_L}{1+g_{m5}R_L} = \dfrac{12.0}{13.0} = 0.92$

Overall:

$A_{total} = 83 \times 0.92 = 76$ (SPICE: 76)

R_L carries DC current $\Rightarrow$ boosts I_{D5} and g_{m5} $\Rightarrow$ better buffer gain.

Theory vs. SPICE: Detailed Comparison

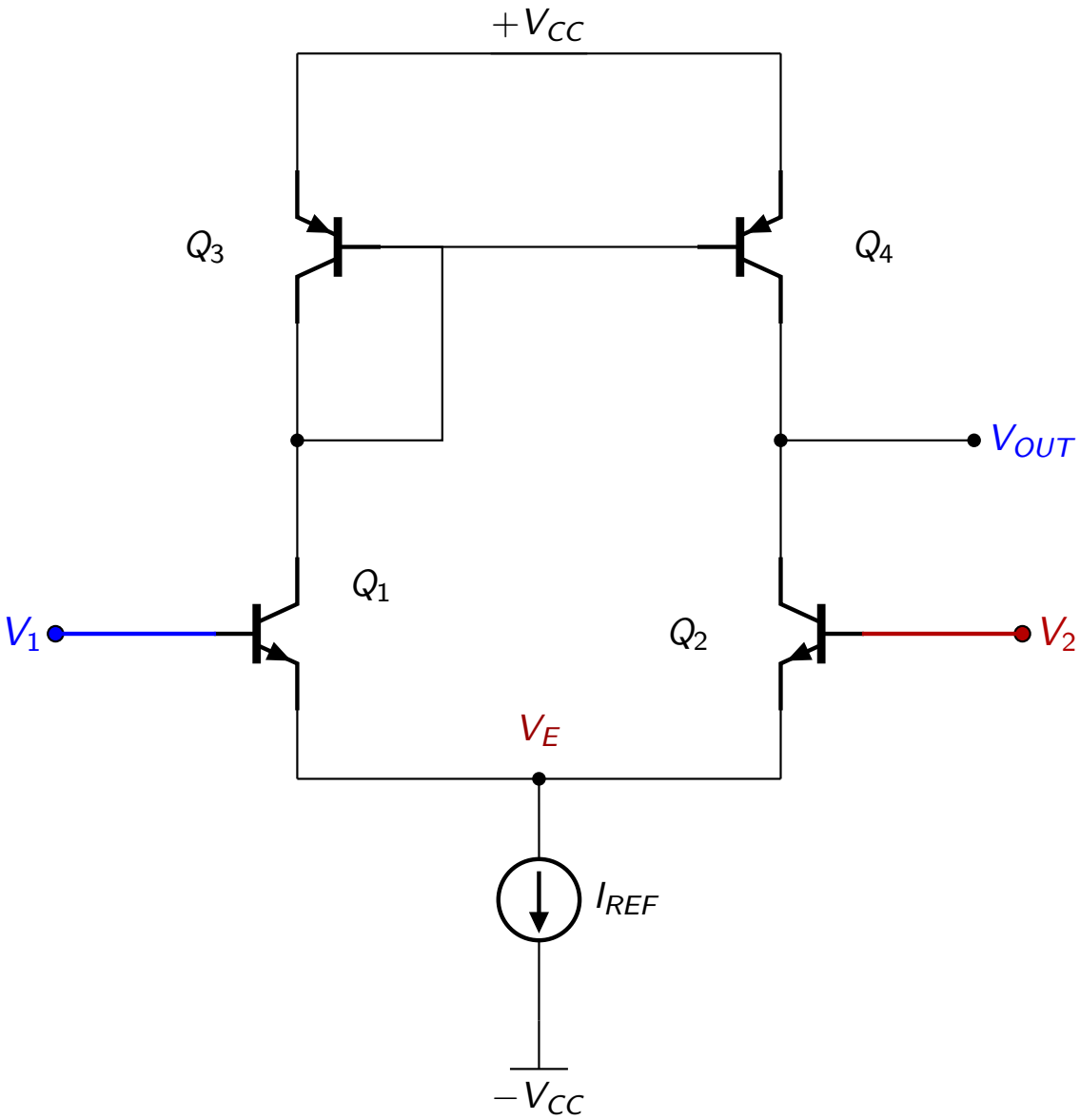
Parameter	Hand Calc	SPICE
Differential Pair		
I_D (M_1/M_2)	450 μA	450 μA
$g_{m,n}$	1.40 mA/V	1.40 mA/V
r_{o2}	111 kΩ	122 kΩ
r_{o4}	111 kΩ	114 kΩ
$r_{o2} \| r_{o4}$	55.5 kΩ	59 kΩ
A_{diff}	78	83
Source Follower Buffer		
V_{out} (DC)	2.5 V	**2.49 V**
$I_{D5} = I_{BIAS} + V_{out}/R_L$	3.4 mA	**3.5 mA**
g_{m5}	12.0 mA/V	**12.0 mA/V**
$g_{m5}R_L$	12.0	12.0
A_{buffer}	0.92	0.92
Overall		
A_{total}	72	**76**

Main error: underestimating V_{out} DC. With actual values, theory matches SPICE within 1%.

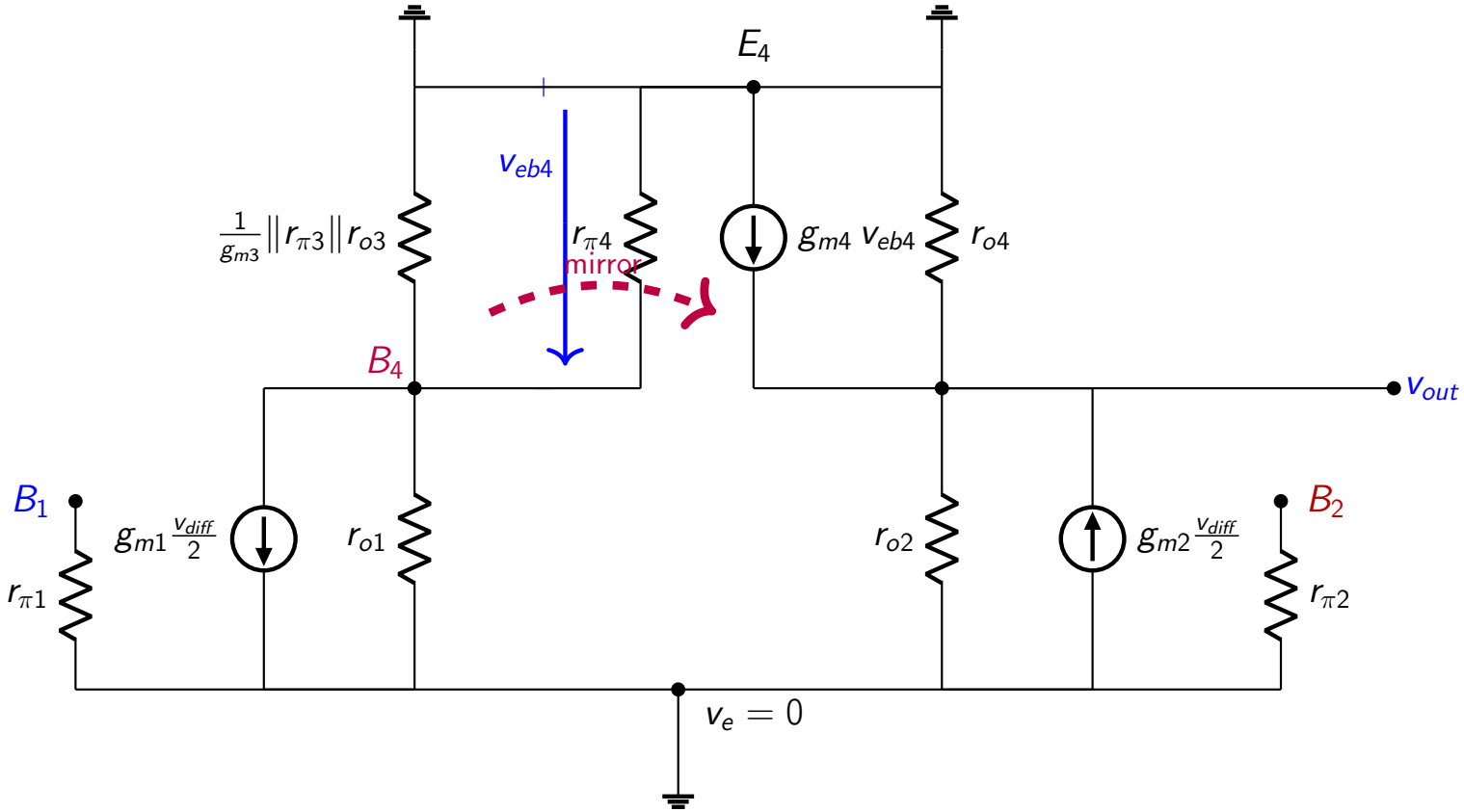
BJT Diff Pair

with PNP Current Mirror Load

BJT Active Load Circuit

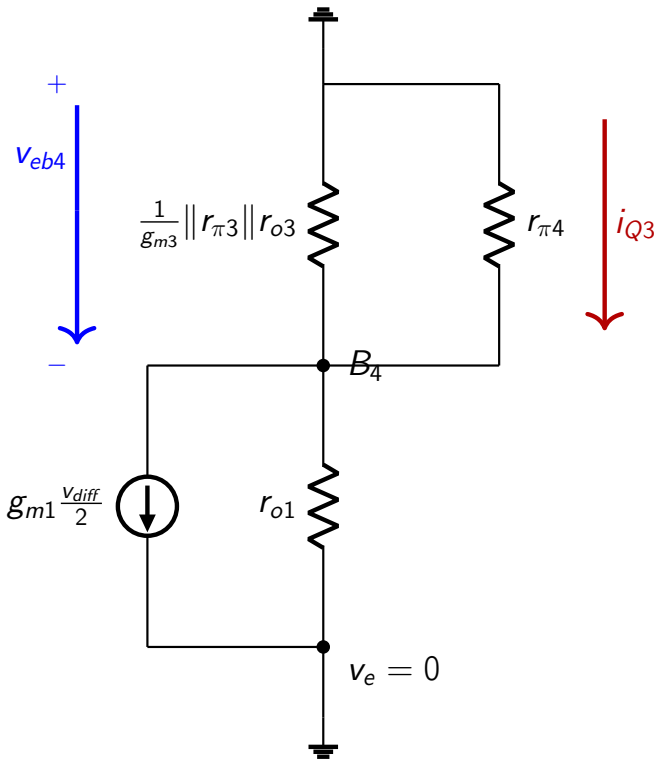


BJT Small-Signal Equivalent Circuit



Same as MOSFET, but r_π from each base to emitter (ground). v_{eb4} replaces v_{sg4}.

BJT Left Half: Q_1 and Q_3



Example: $I_C = 450\ \mu$A, $\beta = 100$, $V_A = 50$ V

$1/g_{m3}$	**58** Ω
$r_{\pi 3}$	5.8 kΩ
r_{o3}	111 kΩ
$r_{\pi 4}$	5.8 kΩ

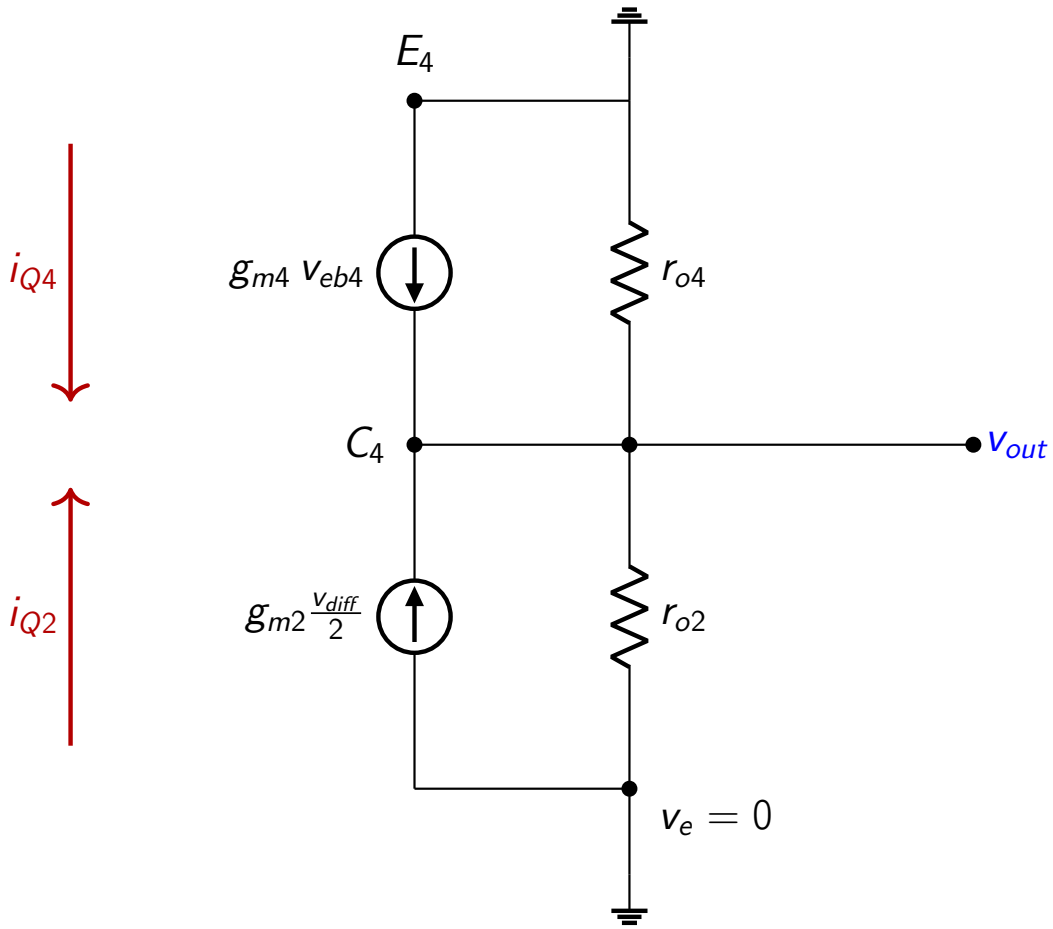
All four in parallel:

$$\frac{1}{g_{m3}} \| r_{\pi 3} \| r_{o3} \| r_{\pi 4} \approx 58 \| 5.8\text{k} \| 111\text{k} \| 5.8\text{k} \approx \mathbf{57}\ \Omega \approx \frac{1}{g_{m3}}$$

$1/g_{m3}$ dominates: r_π is 100× larger, r_o is 1900× larger.

$$v_{eb4} \approx g_{m1} \frac{v_{diff}}{2} \cdot \frac{1}{g_{m3}} = \frac{v_{diff}}{2} \qquad \text{(matched: } g_{m1} = g_{m3}\text{)}$$

BJT Right Half: Q_2 and Q_4



$$i_{Q4} = g_{m4}\, v_{eb4} = g_{m4}\frac{v_{diff}}{2} \qquad i_{Q2} = g_{m2}\frac{v_{diff}}{2}$$

BJT Active Load Gain

The analysis is identical to the MOSFET case:

Virtual ground at $v_e = 0$ (same symmetry argument)

Signal current $\Delta i = g_m v_{diff}/2$ steered by Q_1/Q_2

Q_3/Q_4 mirror doubles the current at the output node

Net signal current at output: $g_m v_{diff}$

Output resistance: $r_{o2} \| r_{o4}$

$$\boxed{A_{diff} = g_m (r_{o2} \| r_{o4})}$$

Same form as MOSFET. BJT has higher $g_m = I_C/V_T$ but typically comparable $r_o = V_A/I_C$, so BJT active-load gains are also very high.

BJT Input Impedance

The differential input impedance is seen looking into the bases of Q_1 and Q_2.

BJT bases draw **finite** base current: $I_B = I_C/\beta$

Small-signal input resistance per transistor: $r_\pi = \beta/g_m = V_T/I_B$

Looking into both bases differentially:

$$\boxed{R_{in,diff} = 2\,r_\pi = \frac{2\,\beta}{g_m}}$$

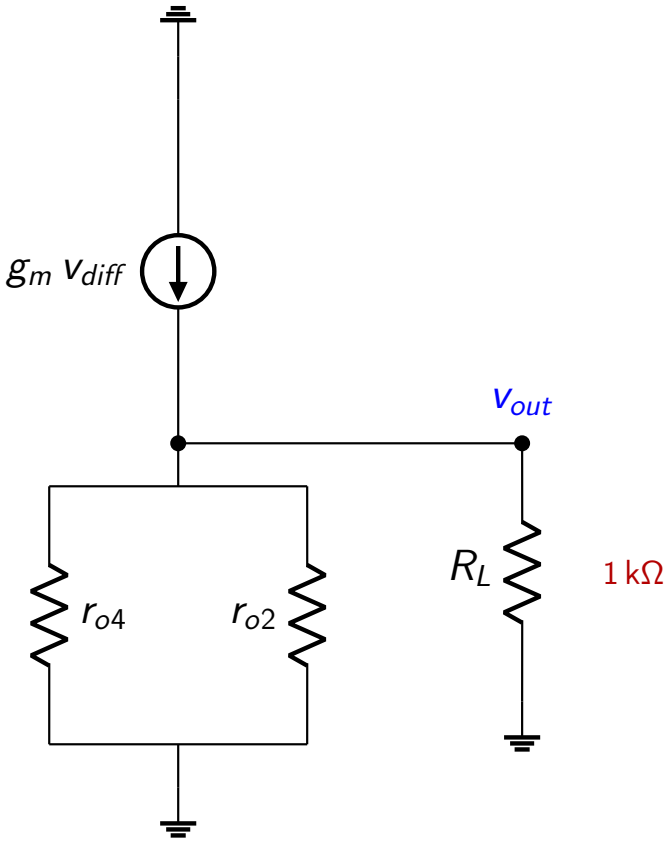
Example: $\beta = 100$, $I_C = 450\ \mu$A, $g_m = I_C/V_T = 17.3$ mA/V

$r_\pi = 100/17.3\text{m} = 5.8\ \text{k}\Omega$, $\quad R_{in,diff} = 11.6\ \text{k}\Omega$

Finite, but still large — compare to MOSFET ($R_{in} = \infty$)

BJT input impedance is finite ($2r_\pi$) but typically >10 kΩ.
MOSFET wins here with $R_{in} = \infty$.

BJT: What Happens with a Load Resistor?



Same problem as MOSFET:

With R_L at the output:

$$A_{diff} = g_m\,(R_L \| r_{o2} \| r_{o4}) \approx g_m\, R_L$$

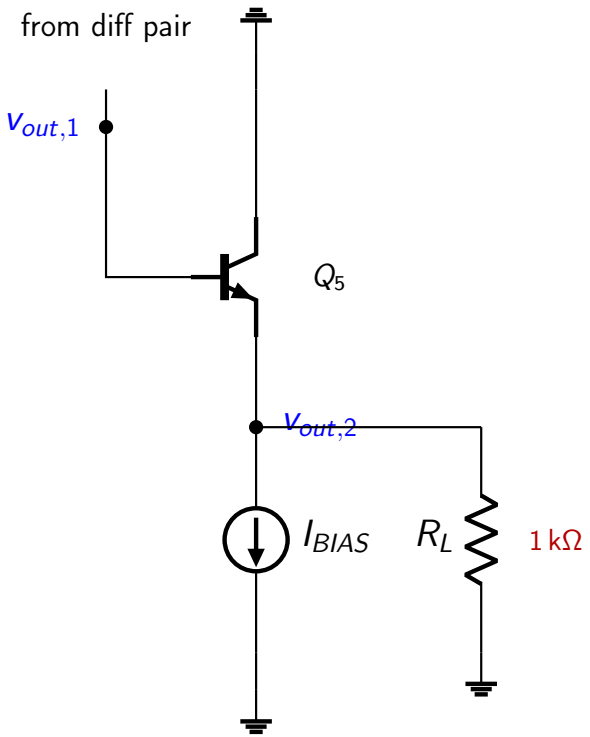
Example: $I_C = 450\ \mu$A, $g_m = I_C/V_T = 17.3$ mA/V

$A_{diff} \approx 17.3 \times 1 = 17.3$ vs. $g_m r_o/2$ (no load)

BJT has higher g_m than MOSFET at same I_C, so $g_m R_L$ is larger, but still far below the open-loop gain.

R_L destroys the high gain. Solution: add a **common-collector** (emitter follower) buffer.

BJT: Buffer with an Emitter Follower



Common-collector (emitter follower):

Input Z: $r_{\pi 5}(1 + g_{m5}R_L) \approx \beta R_L$ (high)

Output Z: $\approx 1/g_{m5}$ (low)

$g_{m5} = I_{C5}/V_T$

With $I_{C5} = 1$ mA: $g_{m5} = 38.5$ mA/V

$g_{m5}R_L = 38.5 \gg 1$

Buffer gain: $\dfrac{g_{m5}R_L}{1 + g_{m5}R_L} = \dfrac{38.5}{39.5} = 0.97$

Overall:

$$A_{total} = g_m(r_{o2} \| r_{o4}) \times 0.97$$

BJT buffer is **better** than MOSFET buffer because $g_m = I_C/V_T$ is much higher for the same bias current.

BJT emitter follower: $g_m R_L \gg 1 \Rightarrow$ buffer gain ≈ 1. Nearly lossless!

BJT: Theory vs. SPICE

	Formula	Thy	SPICE
No load	$g_m(r_{o2} \| r_{o4})$	1006	**1004**
$R_L = 1\,\text{k}$	$g_m R_L$	17.1	**17.4**
Buffered	$g_m(r_{o2} \| r_{o4} \| R_{in5}) \cdot A_{buf}$	624	**631**

Key values: $I_C = 450\ \mu\text{A}$, $g_m = 17.2\ \text{mA/V}$, $r_o \approx 117\ \text{k}\Omega$

Why buffered gain $<$ no-load gain:

Q_5 input impedance: $R_{in5} = r_{\pi 5}(1 + g_{m5} R_L) = 103\ \text{k}\Omega$

This **loads** the diff pair: $r_{o2} \| r_{o4} \| R_{in5} = 37\ \text{k}\Omega$ (was 59 kΩ)

Diff pair gain drops from 1006 to 640

Buffer gain $= 0.975 \Rightarrow A_{total} = 640 \times 0.975 = 624$

Unlike MOSFET ($R_{in} = \infty$), the BJT buffer loads the diff pair through $r_{\pi 5}$.
Still much better than no buffer: 631 vs. 17.4.

Lecture 20 Summary

Replacing R_D with a **PMOS current mirror** creates an **active load**

M_3 (diode-connected) senses current from M_1; M_4 mirrors it to the output

The mirror **doubles** the signal current at the output node

Output is now **single-ended** (taken from M_2/M_4 drain)

Gain: $A_{diff} = g_m (r_{o2} \| r_{o4})$

Since $r_o \gg R_D$, the active load gives **much higher gain**

A **source follower** (MOSFET) or **emitter follower** (BJT) buffers the output to drive low-impedance loads

Same analysis applies to BJT with PNP mirror load

The active-load diff pair is the input stage of an **op amp**