EE461g: Introduction to Electronic Circuits

Lecture 22 — BJT Diff Pair: Answering Student Questions

Dr. Lau

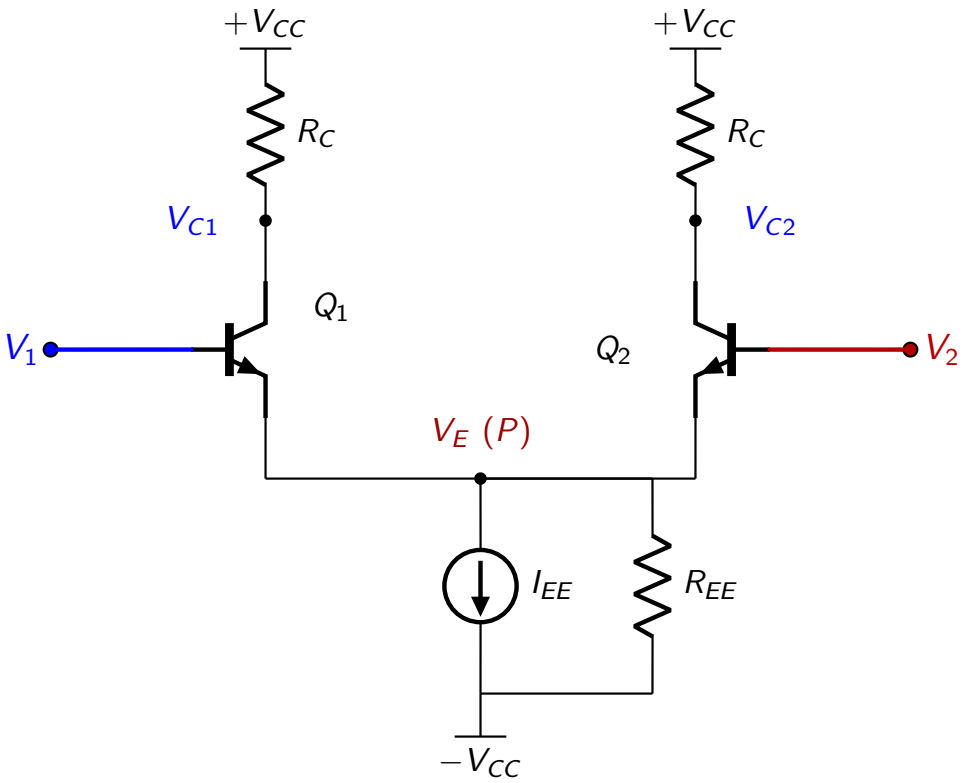
University of Kentucky

Three Questions from a Student

1. **The tail.** "I'm unsure if the tail current source should be included in the small-signal circuit."
2. **The virtual ground.** "Proving that the emitter node v_e (node P) is a virtual ground is not clear. The book says $g_{m1} \approx g_{m2}$ and $v_{in1} \approx v_{in2}$ — is that an approximation?"
3. **The goal.** "What value am I actually trying to find?"

We will answer these three questions in order, then do the full analysis.

Recall: the BJT Diff Pair (Lecture 19, slide 23)



Same topology as Lecture 19, with an explicit tail resistor R_{EE} next to I_{EE}.

Q1: Does the tail current source appear in small-signal?

Rule: convert each DC element to its small-signal equivalent.

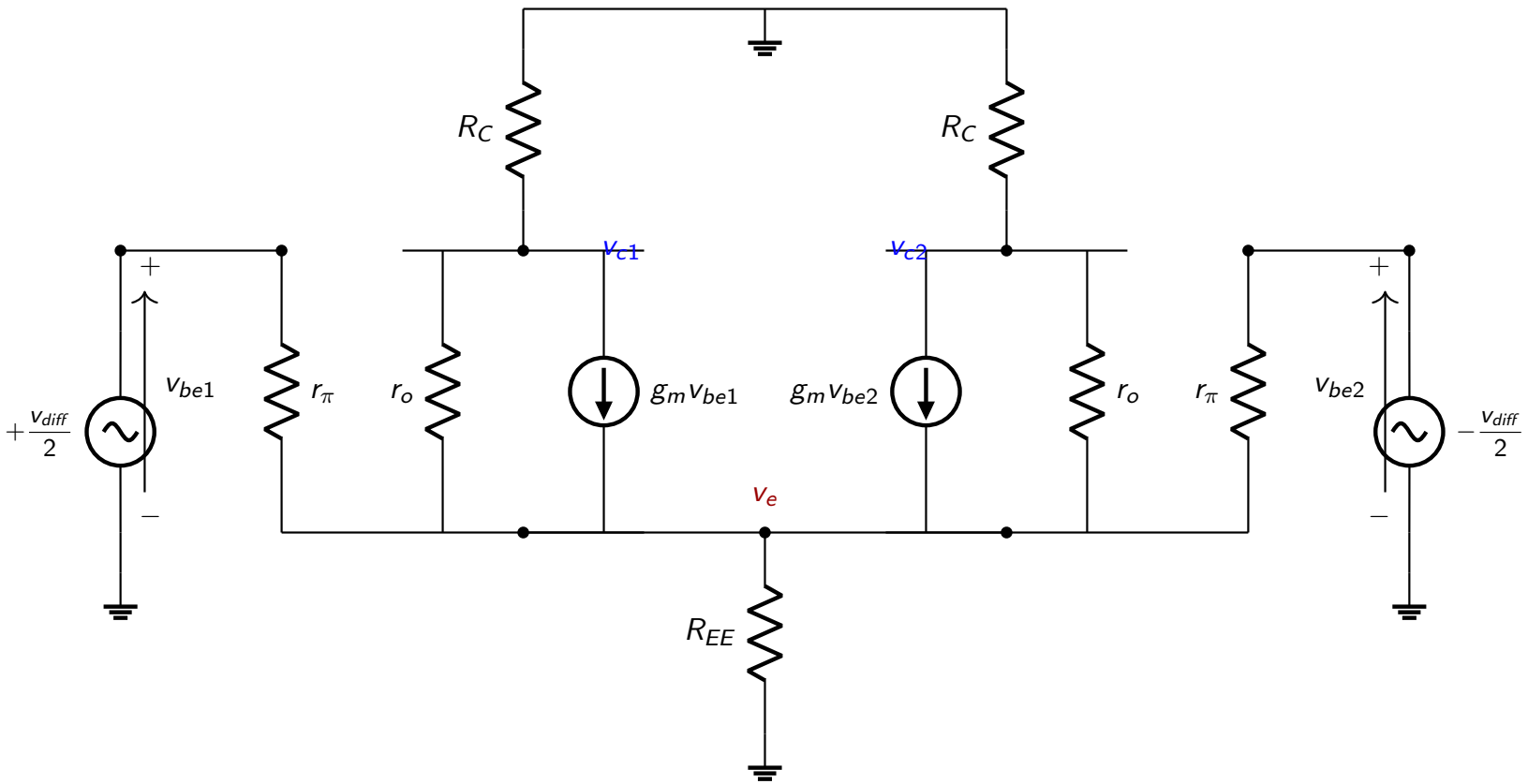
- DC voltage sources ($+V_{CC}$, $-V_{CC}$) $\rightarrow$ **short to ground**
- DC (ideal) current sources (I_{EE}) $\rightarrow$ **open circuit**
- Resistors stay as resistors

So the ideal tail current source I_{EE} disappears.

But if a tail *resistor* R_{EE} is present (in parallel with I_{EE}, or the output resistance of a real current source), it **stays** — connected from v_e to ground (since $-V_{CC} \rightarrow 0$).

This is the case that worried the student's circuit — we will show next that **it does not change the virtual-ground result.**

BJT Small-Signal Model with R_{EE}



I_{EE} is gone (open). R_{EE} remains from v_e to ground. Everything else matches Lecture 19, slide 25.

Q2: What the book is *really* saying

The textbook writes $g_{m1} \approx g_{m2}$ and $v_{in1} \approx v_{in2}$, which sounds like an approximation. Let us untangle the two statements:

$g_{m1} = g_{m2}$ is **exact** by the *matched device* assumption.

Both transistors carry $I_C = I_{EE}/2$, so $g_m = I_C/V_T$ is identical. Same for r_π and r_o.

$v_{in1} \neq v_{in2}$ in general. What is equal is their *common-mode* part.

We decompose: $v_{in1} = V_{CM} + \frac{v_{diff}}{2}$, $v_{in2} = V_{CM} - \frac{v_{diff}}{2}$.

The virtual ground at v_e is **not** an approximation. It is a consequence of **symmetry** applied to the **differential** (antisymmetric) input.

KCL at the Emitter Node v_e

Let v_e be the (unknown) small-signal voltage at the emitter node. Write KCL as the sum of currents **leaving** v_e equals zero. Six branches touch v_e:

$$\underbrace{\frac{v_e - v_{be1\,top}}{r_\pi}}_{\text{into } r_{\pi 1}} + \underbrace{\frac{v_e - v_{be2\,top}}{r_\pi}}_{\text{into } r_{\pi 2}} + \underbrace{\frac{v_e - v_{c1}}{r_o}}_{\text{into } r_{o1}} + \underbrace{\frac{v_e - v_{c2}}{r_o}}_{\text{into } r_{o2}}$$

$$- \underbrace{g_m v_{be1}}_{\text{from Q1's CCS}} - \underbrace{g_m v_{be2}}_{\text{from Q2's CCS}} + \underbrace{\frac{v_e}{R_{EE}}}_{\text{into } R_{EE}} = 0.$$

With $v_{be1} = (+v_{diff}/2) - v_e$ and $v_{be2} = (-v_{diff}/2) - v_e$:

$$\frac{-v_{be1}}{r_\pi} + \frac{-v_{be2}}{r_\pi} + \frac{v_e - v_{c1}}{r_o} + \frac{v_e - v_{c2}}{r_o} - g_m v_{be1} - g_m v_{be2} + \frac{v_e}{R_{EE}} = 0.$$

Now evaluate each term under the antisymmetric drive.

Term-by-Term: Each Pair Cancels

Use antisymmetry. Let $v_{be1} = -v_{be2}$. Then by symmetry $v_{c1} = -v_{c2}$. Pair the terms:

r_π pair:

$$\frac{-v_{be1}}{r_\pi} + \frac{-v_{be2}}{r_\pi} = \frac{-(v_{be1} + v_{be2})}{r_\pi} = \frac{-(v_{be1} - v_{be1})}{r_\pi} = 0.$$

g_m (CCS) pair:

$$-g_m v_{be1} - g_m v_{be2} = -g_m(v_{be1} + v_{be2}) = 0.$$

r_o pair:

$$\frac{v_e - v_{c1}}{r_o} + \frac{v_e - v_{c2}}{r_o} = \frac{2v_e - (v_{c1} + v_{c2})}{r_o} = \frac{2v_e}{r_o}.$$

KCL collapses to:

$$\frac{2v_e}{r_o} + \frac{v_e}{R_{EE}} = 0 \quad \Longrightarrow \quad v_e\left(\frac{2}{r_o} + \frac{1}{R_{EE}}\right) = 0 \quad \Longrightarrow \quad \boxed{v_e = 0.}$$

Consequence: R_{EE} Carries No Signal Current

With $v_e = 0$:

$$i_{R_{EE}} = \frac{v_e}{R_{EE}} = 0, \qquad i_{r_{o1}} + i_{r_{o2}} = \frac{-v_{c1} - v_{c2}}{r_o} = 0,$$

$$i_{r_{\pi 1}} = -\frac{v_{be1}}{r_\pi} = -\frac{v_{diff}}{2r_\pi}, \qquad i_{r_{\pi 2}} = -\frac{v_{be2}}{r_\pi} = +\frac{v_{diff}}{2r_\pi}.$$

Currents into v_e from Q1's side are exactly matched by equal currents *out* through Q2's side. Nothing leaks into R_{EE}.

The virtual ground $v_e = 0$ is exact, **not** an approximation, and holds **with or without** R_{EE}.

Q3: What are we solving for?

The value of a differential amplifier is its **differential gain**:

$$A_d \equiv \frac{v_{out}}{v_{diff}} = \frac{v_{c2} - v_{c1}}{v_1 - v_2}.$$

Secondary quantities that are often asked for:

- **Single-ended gain**: v_{c1}/v_{diff} or v_{c2}/v_{diff}
- **Differential input resistance**: R_{id} looking into the two bases
- **Common-mode gain** A_{cm} and **CMRR** $= |A_d/A_{cm}|$

For now, the goal is A_d. Once we know $v_e = 0$, each side reduces to a **common-emitter amplifier** — the rest is bookkeeping.

Half-Circuit Analysis

With $v_e = 0$, the emitter is grounded and the two halves decouple. Consider the left side:

$$v_{be1} = +\frac{v_{diff}}{2}.$$

The collector current source delivers $g_m v_{be1}$ into the parallel combination $R_C \parallel r_o$ (to AC ground at the top rail):

$$v_{c1} = -g_m v_{be1} (R_C \parallel r_o) = -g_m (R_C \parallel r_o) \frac{v_{diff}}{2}.$$

By symmetry, the right side gives

$$v_{c2} = -g_m (R_C \parallel r_o) \left(-\frac{v_{diff}}{2}\right) = +g_m (R_C \parallel r_o) \frac{v_{diff}}{2}.$$

Each collector sees half of v_{diff} through a CE-amp gain of $-g_m(R_C \parallel r_o)$.

Differential Gain A_d

The differential output is

$$v_{out} = v_{c2} - v_{c1} = g_m(R_C \parallel r_o)\, v_{diff}.$$

So

$$\boxed{A_d = \frac{v_{out}}{v_{diff}} = g_m\,(R_C \parallel r_o)}$$

If $r_o \gg R_C$ (very common): $A_d \approx g_m R_C$.

Single-ended outputs (e.g. you only tap v_{c2}):

$$\frac{v_{c2}}{v_{diff}} = +\tfrac{1}{2}\, g_m(R_C \parallel r_o), \qquad \frac{v_{c1}}{v_{diff}} = -\tfrac{1}{2}\, g_m(R_C \parallel r_o).$$

Same form as the MOSFET diff pair. BJT just uses $g_m = I_C/V_T$ instead of $g_m = 2I_D/V_{OV}$.

Differential Input Resistance

Looking into the two bases (from one base, through $r_{\pi 1}$, across $v_e = 0$, through $r_{\pi 2}$, to the other base):

$$R_{id} = r_{\pi 1} + r_{\pi 2} = 2\, r_{\pi}.$$

This is the **only** place where finite r_{π} shows up in the differential answer — it does not appear in A_d (because v_{be} is set directly by the source with $v_e = 0$).

Contrast with MOSFET: $r_{\pi} \to \infty$ for a MOSFET, so $R_{id} \to \infty$ there.

Answers to the Student's Questions

1. **Tail in small-signal.**
   Ideal $I_{EE} \rightarrow$ open. A tail resistor R_{EE} (or real current-source output resistance) stays, hooked from v_e to ground (since $-V_{CC} \rightarrow 0$).

2. **Virtual ground at v_e.**
   Not an approximation. From *matched devices* + *antisymmetric drive*, symmetry forces every signal current leaving v_e through Q1's side to be matched by one entering through Q2's side. R_{EE} sees $v_e = 0$ and carries no signal current.

3. **What to solve for.**
   Differential gain $A_d = v_{out}/v_{diff} = g_m(R_C \parallel r_o)$. With $v_e = 0$, each half is a common-emitter amplifier driven by $\pm v_{diff}/2$.

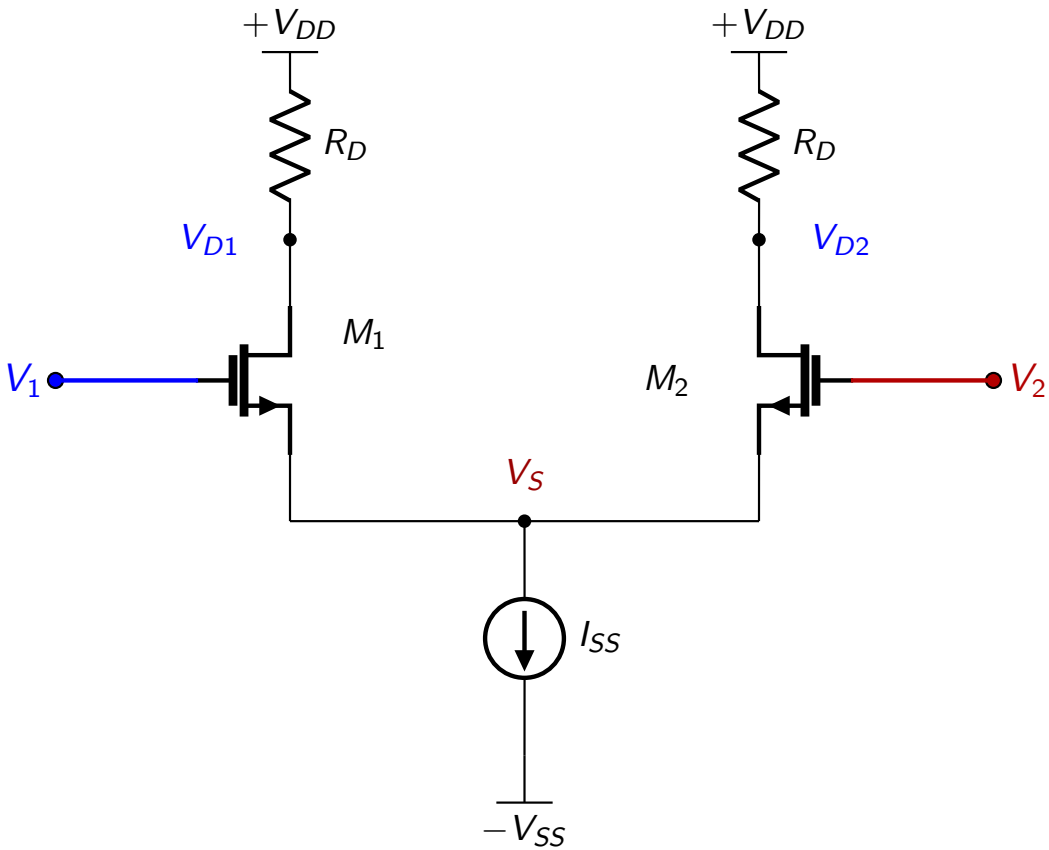
Key takeaway: **symmetry does the heavy lifting**. Everything connected from v_e to ground drops out for differential analysis.

Homework Circuit

MOSFET Diff Pair

$\rightarrow$ Active Load

Starting Point: NMOS Diff Pair with R_D Loads



Familiar topology (Lecture 19). Differential gain:

$$A_d = g_m (R_D \parallel r_o) \approx g_m R_D.$$

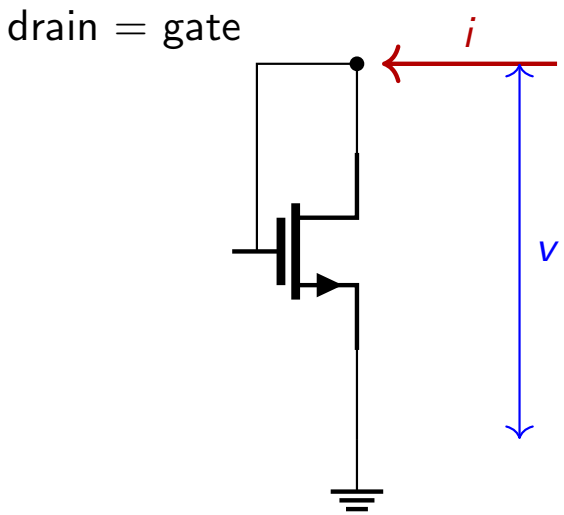
Why Replace R_D?

Problem with R_D. To get decent gain $A_d = g_m R_D$, we need a *large* R_D. But:

- Each drain carries $I_{SS}/2$, so the DC drop across R_D is $\frac{I_{SS}}{2} R_D$.
- Large R_D plus useful bias $\Rightarrow$ big voltage drop $\Rightarrow$ low output swing or huge V_{DD}.
- On-chip, large resistors are expensive (area) and inaccurate ($\pm 20\%$).

Idea. Replace each R_D with a transistor biased to look like a *small-signal* resistor, while setting its own DC current. The simplest choice: a **diode-connected NMOS** (gate shorted to drain).

Diode-Connected NMOS: Small-Signal Resistance



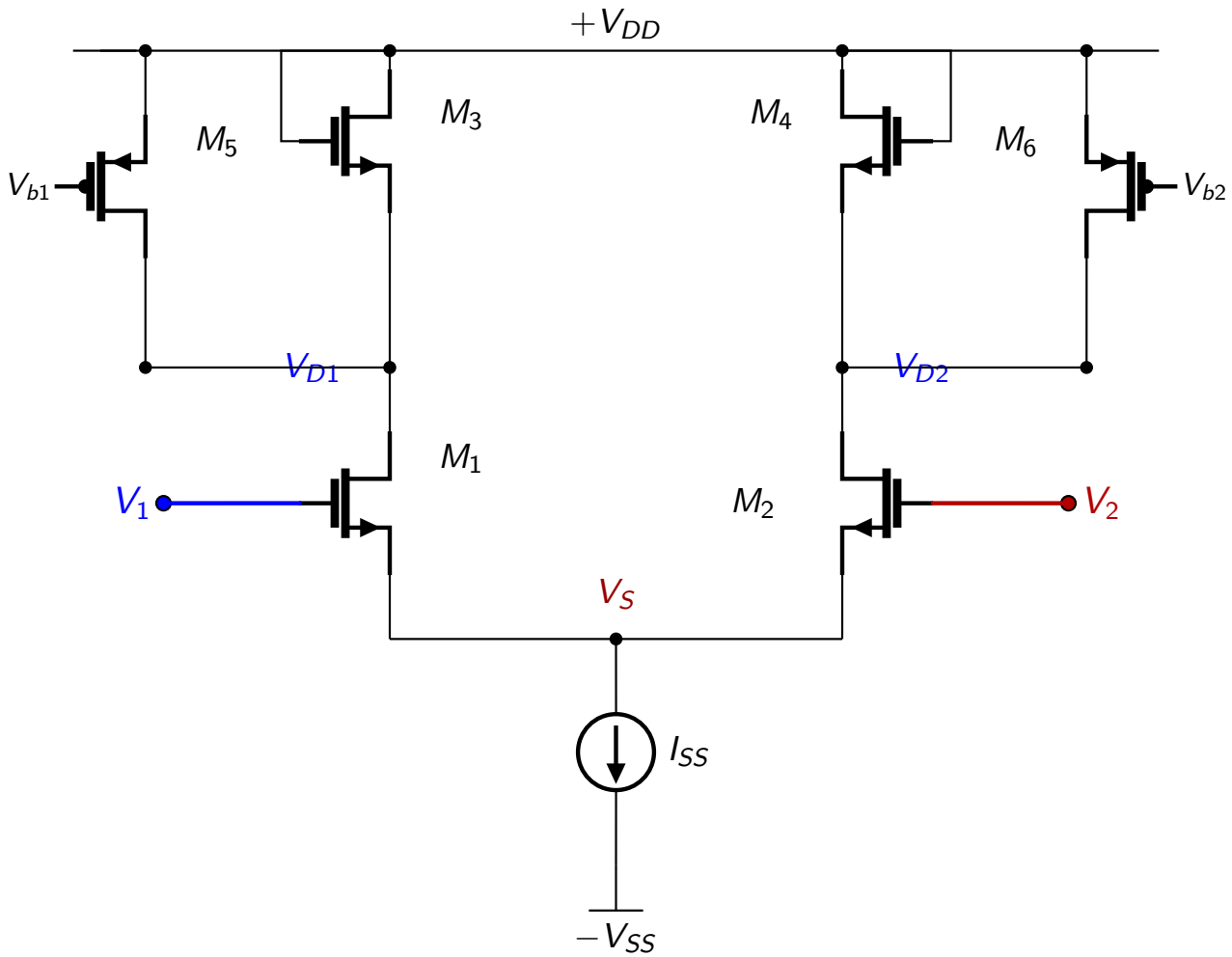
Because $V_{GS} = V_{DS}$, the device is always in saturation (as long as $V_{GS} > V_t$).
Small-signal model:

$$i = g_m v_{gs} + \frac{v_{ds}}{r_o} = \left(g_m + \frac{1}{r_o}\right) v$$

$$R_{diode} = \frac{v}{i} = \frac{1}{g_m + 1/r_o} \approx \frac{1}{g_m}.$$

A diode-connected MOSFET looks like a small-signal resistor of value $\boxed{1/g_m}$ (ignoring r_o).

Replace R_D with Diode-Connected NMOS Loads



Each R_D replaced by a diode-connected NMOS (M_3, M_4) — gate shorted to drain.

Gain with Diode-Connected Loads

Each drain node now sees, to small-signal ground (V_{DD}):

$$R_{load} = r_{o1}(\text{of } M_1) \parallel \underbrace{\frac{1}{g_{m3}} \parallel r_{o3}}_{\text{diode-connected } M_3} \approx \frac{1}{g_{m3}}.$$

(assuming $1/g_{m3} \ll r_{o1}, r_{o3}$, which is the usual case).

Half-circuit gain from $+v_{diff}/2$ to v_{d1}:

$$v_{d1} = -g_{m1} R_{load} \frac{v_{diff}}{2} \approx -\frac{g_{m1}}{g_{m3}} \frac{v_{diff}}{2}.$$

Symmetric for the other side, so the differential output is:

$$\boxed{A_d = \frac{v_{d2} - v_{d1}}{v_{diff}} = \frac{g_{m1}}{g_{m3}}}$$

Gain is a **ratio of transconductances** — set by device sizes and currents, not by resistor values. Great for IC design.

g_{m1}/g_{m3} in Terms of Device Sizes

For a square-law NMOS in saturation, $g_m = \sqrt{2k'_n\,(W/L)\,I_D}$.

Both M_1 and M_3 carry the same drain current (series stack): $I_D = I_{SS}/2$. So:

$$\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{(W/L)_1}{(W/L)_3}}.$$

Consequences:

- Gain is set by a *geometric ratio* — well-matched, process-insensitive.
- Typical designs use $(W/L)_1 \gg (W/L)_3$ to boost gain; practical limit is a few $\times 10$ before secondary effects dominate.
- Gain is **independent of bias current** (to first order) — nice for low-power biasing.

Trade-off: the gain achievable with diode loads is modest. To push higher, swap the top for a **current-mirror** load — that is the next step.