EE461g: Introduction to Electronic Circuits

Lecture 23 — BJT Diff Pair with Single-PNP Active Load

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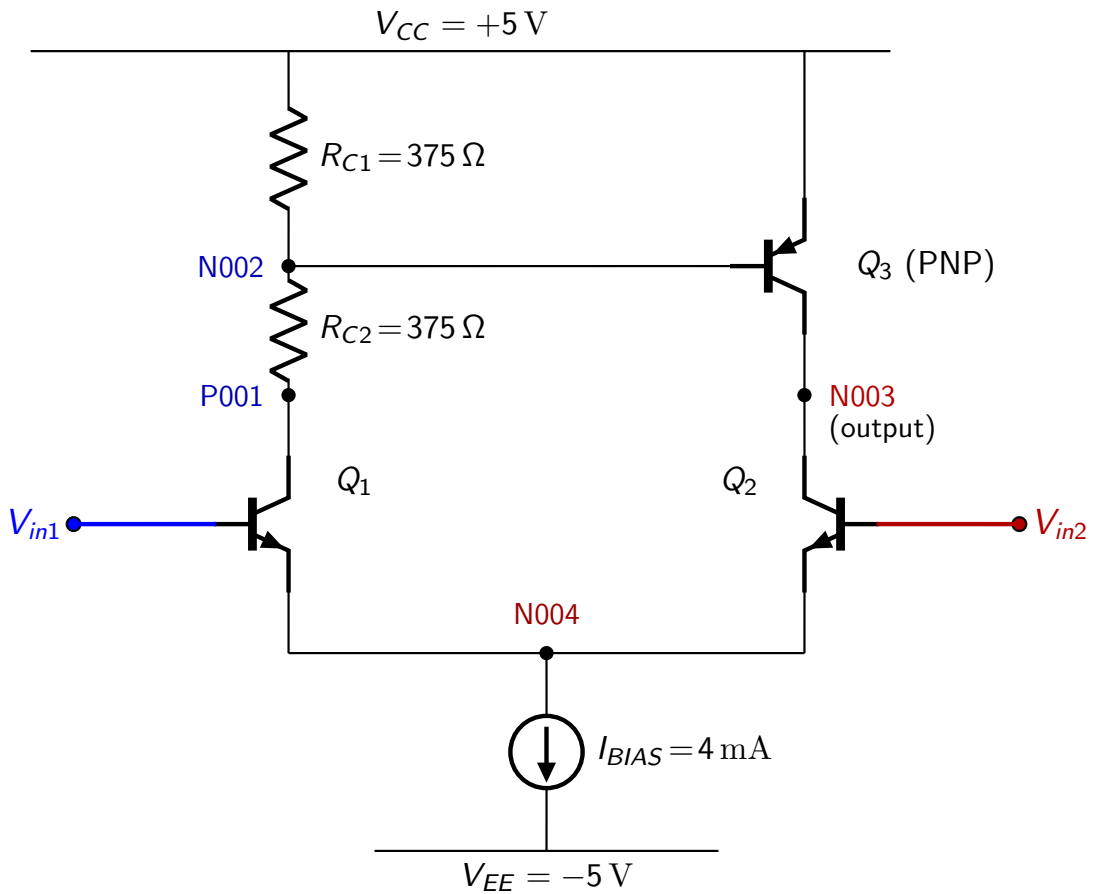
Today's Circuit: Diff Pair with PNP Active Load



NPN diff pair Q_1, Q_2 with a $4\,\mathrm{mA}$ tail. Q_3 is a single-PNP active load whose V_{BE} is set by the drop across R_{C1}.

The SPICE Netlist (As Given)

```
RC1  N001  N002  375
VCC  N001  0  5
RC2  N002  P001  375
Q1   P001  V1    N004  0  NPN
Q2   N003  V2    N004  0  NPN
Q3   N003  N002  N001  0  PNP
IBias  N004  P002  .004
V1   0     P002  5
.model  NPN  NPN
.model  PNP  PNP
.lib  C:\Users\mlhar\AppData\Local\LTspice\lib\cmp\standard.bjt
.op
.backanno
.end
```

Two problems will keep this from giving useful results – next slide.

Two Problems With This Netlist

1. **Floating bases.**
   The Q1/Q2 base nodes are named `V1` and `V2`, but *no voltage sources drive them*. With nothing tying these to a known potential, `.op` either fails or returns garbage.

2. **Name collision.**
   `V1` is used both as a *node* (Q1's base) and as a *device* (the $-5\,\mathrm{V}$ rail source). LTspice keeps device and node namespaces separate, so it parses, but it is fragile and misleading.

Fix: add input sources `Vin1`, `Vin2` on the bases, and rename the rail source from `V1` to `VEE`.

DC Operating Point: Diff Pair Side

Symmetric drive: set $V_{in1} = V_{in2} = 0$ (common-mode at ground).

Tail splits evenly between Q_1 and Q_2:

$$I_{C1} = I_{C2} \approx \tfrac{1}{2} I_{BIAS} = 2\,\mathrm{mA}.$$

Drop across R_{C2} (carries I_{C1}):

$$V_{R_{C2}} = (2\,\mathrm{mA})(375\,\Omega) = 0.75\,\mathrm{V} \quad \Rightarrow \quad V(\mathrm{P001}) = V(\mathrm{N002}) - 0.75\,\mathrm{V}.$$

Drop across R_{C1} (carries $I_{C1} + I_{B3} \approx I_{C1}$):

$$V_{R_{C1}} \approx (2\,\mathrm{mA})(375\,\Omega) = 0.75\,\mathrm{V} \quad \Rightarrow \quad V(\mathrm{N002}) \approx 5 - 0.75 = 4.25\,\mathrm{V}.$$

The drop across R_{C1} *is* V_{BE} of Q_3. Setting $R_{C1} I_{C1} = V_{BE3} \approx 0.7$–$0.75\,\mathrm{V}$ pins the bias.

DC Currents: Matched BJTs, $\beta = 50$, $I_S = 6 \times 10^{-16}$ A

Assumptions: all three BJTs matched, $\beta = 50$, $I_S = 6 \times 10^{-16}\,\text{A}$, $V_T = 26\,\text{mV}$.

Reasoning:

- Symmetric drive: tail KCL $\Rightarrow I_{E1} = I_{E2} = I_{BIAS}/2 = 2.000\,\text{mA}$.
- Each device: $I_C = \frac{50}{51}(2) = 1.961\,\text{mA}$, $I_B = I_E/51 = 39.2\,\mu\text{A}$.
- KCL at N003 $\Rightarrow I_{C3} = I_{C2} = 1.961\,\text{mA}$.
- $|V_{BE}| = V_T \ln(I_C/I_S) = 0.026 \ln(1.961 \times 10^{-3}/6 \times 10^{-16}) = 0.749\,\text{V}$.

Device	I_B	I_C	I_E	$\lvert V_{BE}\rvert$
Q_1 (NPN)	$39.2\,\mu\text{A}$	$1.961\,\text{mA}$	$2.000\,\text{mA}$	$0.749\,\text{V}$
Q_2 (NPN)	$39.2\,\mu\text{A}$	$1.961\,\text{mA}$	$2.000\,\text{mA}$	$0.749\,\text{V}$
Q_3 (PNP)	$39.2\,\mu\text{A}$	$1.961\,\text{mA}$	$2.000\,\text{mA}$	$0.749\,\text{V}$

Resistor currents: $I_{R_{C2}} = I_{C1} = 1.961\,\text{mA}$, $I_{R_{C1}} = I_{R_{C2}} - I_{B3} = 1.922\,\text{mA}$.

Matched devices carry identical I_C, so all three have $|V_{BE}| = 0.749\,\text{V}$.

DC Node Voltages

$|V_{BE}| = 0.749\,\mathrm{V}$ across every junction; inputs at DC ground ($V_{in1} = V_{in2} = 0$).

Key relations: $V(\mathrm{N004}) = V_{in1} - V_{BE} = -0.749\,\mathrm{V}$;
$V(\mathrm{N002}) = V_{CC} - |V_{BE3}| = 4.251\,\mathrm{V}$; $V(\mathrm{P001}) = V(\mathrm{N002}) - I_{C1}R_{C2} = 3.516\,\mathrm{V}$.

Node	Description	Voltage
0	ground (reference)	$0.000\,\mathrm{V}$
N001	V_{CC} rail	$+5.000\,\mathrm{V}$
P002	V_{EE} rail	$-5.000\,\mathrm{V}$
V1	Q_1 base (V_{in1})	$0.000\,\mathrm{V}$
V2	Q_2 base (V_{in2})	$0.000\,\mathrm{V}$
N004	shared emitter Q_1, Q_2	$-0.749\,\mathrm{V}$
N002	Q_3 base, R-stack midpoint	$+4.251\,\mathrm{V}$
P001	Q_1 collector	$+3.516\,\mathrm{V}$
N003	output (Q_2, Q_3 collector)	high-Z

No Early effect $\Rightarrow$ $V(\mathrm{N003})$ is not pinned by DC analysis. SPICE may rail it unless V_{AF} is added to the model.

Q_3 Provides the High-Impedance Output

At node **N003**, two collectors meet:

- Q_2's collector (NPN) pulls current *down* (toward the tail).
- Q_3's collector (PNP) pushes current *up* (from V_{CC}).

For DC balance: $I_{C3} = I_{C2}$. The bias loop self-adjusts $V(\mathrm{N002})$ until this holds.

When V_{in1} rises slightly (differentially):

- I_{C1} rises $\Rightarrow$ more drop across R_{C1} $\Rightarrow$ V_{BE3} rises $\Rightarrow$ I_{C3} rises.
- Simultaneously, I_{C2} falls (tail is fixed).
- Q_3 pushes *more* into N003 while Q_2 pulls *less* out $\Rightarrow$ output swings up.

Q_3 acts as a **single-transistor current mirror**: it copies (and amplifies) Q_1's current change into Q_2's collector node.

Why a Single PNP Instead of a Two-PNP Mirror?

Standard active load: two matched PNPs forming a current mirror.

This circuit: one PNP, with R_{C1} developing V_{BE3} from I_{C1}.

Pros

- One transistor, two resistors — very compact.
- Mirror ratio adjustable via R_{C1}/R_{C2}.
- Translinear gain: I_{C3} is exponential in $R_{C1}I_{C1}$.

Cons

- Bias is sensitive: $V_{BE3} = 0.75\,\mathrm{V}$ at $2\,\mathrm{mA}$ requires careful R_{C1} choice.
- Mismatch in V_{BE3} versus the assumed $0.7\,\mathrm{V}$ shows up as bias error.
- Poor PSRR vs. V_{CC}: rail noise feeds into N002.

Corrected Netlist for .op

```
* BJT diff pair with single-PNP active load
RC1  N001  N002  375
RC2  N002  P001  375
VCC   N001  0  5
VEE   P002  0  -5

* --- inputs (was floating in the original) ---
Vin1  V1  0  DC  0
Vin2  V2  0  DC  0

Q1  P001  V1    N004  0  QNPN
Q2  N003  V2    N004  0  QNPN
Q3  N003  N002  N001  0  QPNP
IBias  N004  P002  4m

.model  QNPN  NPN  (IS=1e-16  BF=150  VAF=75)
.model  QPNP  PNP  (IS=1e-16  BF=80   VAF=50)

.op
.end
```

What .op Should Report

With $\beta = 50$, $I_S = 6 \times 10^{-16}\,\mathrm{A}$, $V_{BE} = 0.749\,\mathrm{V}$:

Node / current	Value	Comment
$V(\mathrm{N001})$	$+5.000\,\mathrm{V}$	V_{CC} rail
$V(\mathrm{N002})$	$+4.251\,\mathrm{V}$	$V_{CC} - V_{BE3}$
$V(\mathrm{P001})$	$+3.516\,\mathrm{V}$	N002 $- I_{C1} R_{C2}$
$V(\mathrm{N003})$	high-Z (sensitive)	no Early effect $\Rightarrow$ rail
$V(\mathrm{N004})$	$-0.749\,\mathrm{V}$	one V_{BE} below input
$I(R_{C1})$	$1.922\,\mathrm{mA}$	$I_{C1} - I_{B3}$
$I(R_{C2})$	$1.961\,\mathrm{mA}$	$= I_{C1}$
$I(I_{BIAS})$	$4.000\,\mathrm{mA}$	set by source

$V(\mathrm{N003})$ is the high-impedance output. With matched ideal BJTs and no V_{AF}, expect SPICE to push it to V_{CC} or V_{EE} unless you add Early effect or DC feedback.

Summary

1. **Topology.** Standard NPN diff pair with a $4\,\mathrm{mA}$ tail; the load on Q_2's collector is a single PNP whose V_{BE} comes from the drop across R_{C1}.
2. **Q_3's role.** Acts as a one-transistor current mirror. It pushes a copy of Q_1's current into Q_2's collector node, giving a single-ended high-impedance output at **N003**.
3. **Netlist hygiene.** Drive every base with a source. Avoid reusing names across device and node namespaces (the original had `V1` as both).
4. **Bias check.** For $I_{C1} = 2\,\mathrm{mA}$ and $R_{C1} = 375\,\Omega$, the drop is $0.75\,\mathrm{V}$ — exactly the V_{BE} this PNP needs. The designer chose R_{C1} to match the bias point.

Next time: apply a small differential drive and measure $A_d = v_{N003}/v_{diff}$ to see how much gain the active load buys us.