Large Leakage-Current Reduction of Ultrathin Industrial SiON Wafers Induced by Phonon-Energy-Coupling Enhancement

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Large leakage-current reduction of ultrathin SiO2 due to enhanced phonon-energy coupling has generated extensive interest, and also doubts about its authenticity. It was suggested by researchers in the industry that both current–voltage (I–V) and capacitance–voltage (C–V) curves of the same devices fabricated using a lithographic method can prove its validation. We developed a bilayer resist lithographic method to fabricate Ni-gate metal-oxide-semiconductor capacitors to validate this effect. Experimental I–V and C–V curves, together with C–V curves simulated using the Berkeley Quantum simulator, demonstrate that large leakage-current reduction (∼300%) can be reliably and reproducibly achieved on industrial SiON wafers after proper rapid thermal processing. © 2008 The Electrochemical Society. [DOI: 10.1149/1.2969029] All rights reserved.

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Advanced metal-oxide-semiconductor (MOS) transistors need extremely thin gate dielectrics (<20 Å). Transistors operate in a regime in which direct quantum tunneling current dominates the gate leakage. Currently, the industry uses silicon oxynitride (SiON) as the gate insulator, although alternative high-permittivity (high-k) gate dielectrics such as HfO2 and HfSiON show promise for circumventing the gate leakage problem. However, there must be an interfacial SiO2 layer (5–6 Å) between the high-k dielectric and Si for improving electron mobility. Therefore, any improvement in leakage current of SiO2 or SiON is very helpful to MOS transistors.

Recently, we discovered an effect, phonon-energy coupling enhancement (PECE) using Fourier transform infrared spectroscopy, leading to a reduction in the quantum tunneling current of SiO2 by 2–5 orders of magnitude.1–3 It is suggested that the reduction in tunneling current is probably caused by an energy-band-structure change of SiO2 after proper rapid thermal processing (RTP) due to enhanced phonon-energy coupling between the Si–O rocking mode and the Si–Si transverse optical phonon mode (∼460 cm−1).1–3 Because of the nature of the phonon coupling, any attack of the SiO2 structure by chemicals and plasmas may result in partial loss of the PECE effect.4 Alkaline-based chemicals and plasmas, including commonly used photoresist developers (e.g., MF319) and sputtering deposition, should be avoided.5 In the past, to avoid lithography and sputtering, we patterned Al gate metal by the thermal evaporation of Al through shadow masks. This makes easy controllable results because the area of MOS capacitors varies during evaporation through shadow masks at different angles across a large substrate. In addition, people have doubts about this effect because, in our early publications, we did not show capacitance–voltage (C–V) curves of the same device along with current–voltage (I–V) curves.2,3 It was strongly suggested by researchers in the industry that only both I–V and C–V curves from the same device fabricated using a lithographic method are required to validate the observed effect.

In this article, we present a bilayer resist lithographic method using Ni as a gate metal based on all-organic resists and developer so that physical and chemical processes harmful to the PECE effect can be avoided. We will also show that large leakage-current reduction of industrial SiON wafers (Freescale Semiconductor) can be reliably and reproducibly achieved using this lithographic method.

Experimental

As mentioned previously, alkaline-based chemicals and plasmas are harmful to the PECE effect, causing partial loss of the effect.5 A commonly used developer for a positive resist, Microposit S1800 series, is MF-319. It contains tetramethylammonium hydroxide [(CH3)4N][OH−], an alkaline-based chemical. To avoid alkaline-based developers, SU-8 resist was used as the resist of choice for our lithographic process, because the resist, developer, and remover are all organic-based. In addition, Al is not a good gate metal because Al-gate MOS capacitors with ultrathin oxides (<25 Å) become short-circuited after postmetal anneal at 450°C in forming gas because Al diffuses through the oxide. Considering both conductivity and diffusivity, Ni is the best candidate. However, because of its high melting point, Ni can only be deposited using electron-beam evaporation, where the heat from the source causes a reflow of the SU-8 resist so that the “lift-off” process is very difficult.

A key process step in a successful lift-off process is an undercut resist profile. The solution is to have an intermediate layer between the resist and the substrate to ensure the undercut profile. To fulfill this requirement, we have developed a bilayer resist lift-off process utilizing Microposit S1813 positive resist as the intermediate resist layer shown as Fig. 1. Because the SU-8 2001 developer consists of 98% 1-methoxy-2-propyl acetate (C6H12O3), which is a solvent for the Microposit S1800 series resist, no additional developer is needed to develop the bottom lift-off resist layer (S1800 series resist). The resist, however, has to be “semicured” to ensure that the developer does not completely remove the resist layer. The semicure process is a bake on a hot plate at 130°C for 60 s. The detailed lift-off processes are shown in Fig. 1.

Figure 1. Fabrication steps of Ni-gate Si MOS capacitors using a bilayer resist lift-off procedure, in which SU-8/S1813 double-resist layers are used to form undercut.
Undercut profile

Figure 2. SEM image of the undercut formed by exposure and development of SU-8/S1813 double-resist layers.

Two SiON samples, cut from the same wafer (Freescale Semiconductor), were used. SiON is p-type and contains ~7–9% N with an equivalent oxide thickness (EOT) of 15.5 Å (nominal). One piece was used as a control sample, while the other one was subjected to RTP at 1100°C in helium with ~300 to 600 ppm O₂. To accurately control the oxygen concentration, a trace oxygen analyzer (Alpha Omega Series 3000) with a range of 1 to 10,000 ppm was installed before the inlet of the gas line. The RTP time could be chosen so that the oxide regrowth was ~1 to 2 Å, measured using ellipsometry (J. A. Woollam M3000V). After RTP, both samples were fabricated using the bilayer resist process. The first resist layer, S1813, was spin coated at a speed of 2000 rpm, which was then baked on a hot plate at 130°C. This was followed by a coating of SU-8 2001 resist at 3000 rpm and soft baked on a hot plate at 70 and 120°C for 2 min. After UV exposure, the sample was baked at 70 and 120°C for 2 min. The development of the resist was carried out using SU-8 developer for 60 s, followed by a quick rinse in isopropyl alcohol and drying using a nitrogen blower. The undercut profile is clearly seen in the scanning electron microscope (SEM) image as shown in Fig. 2. A ~100 nm thick Ni film was deposited on the patterned resist by electron-beam evaporation and lifted off in the SU-8 remover (PG) heated at 80 to 100°C. After covering the front electrodes using hard-baked S1813 resist at 140°C for 5 min, the back oxide was completely etched using buffered oxide etch. The final step consisted of removing the protective front resist using Microposite 1165 resist remover and subsequent annealing at 450°C in forming gas for 30 min (5% H₂: 95% N₂).

Results and Discussion

Figure 2 shows an SEM micrograph of the bilayer resist undercut profile obtained in this study. There was intermixing of the resists so that individual resists cannot be distinguished in the SEM image. However, as seen in the figure, an undercut profile was created. In addition to the undercut, another key process step, described as follows, has to be used to ensure a successful lift-off. After development of the bilayer resist, samples have to be loaded into a vacuum chamber in less than 15 min; otherwise, the Ni electrodes peel off during the final lift-off step in photoresist remover PG. The detailed mechanism is not understood yet. It appears that, after development, there may be some organic monolayer still present. After exposure in air for over 20 min, it may react with some element in the air so that it becomes a barrier for the diffusion of Ni to the surface of the oxide on the substrate. If samples are loaded in less than 15 min, Ni atoms can penetrate through the monolayer during E-beam evaporation, so that it adheres very well to the gate dielectric during the final lift-off step.

MOS capacitors were fabricated using this bilayer resist process and their electrical characteristics were measured, including I-V and C-V curves. The nominal diameter of capacitors (dots) on the mask was 150 µm. Because the Ni dots were too big for SEM, we usually measured the actual diameter of the Ni dots using an optical microscope. After lift-off, the actual diameter of the Ni dots is 149 µm, which is in agreement with the SEM photo (slightly less than the nominal diameter on the mask). The area difference between the dot on the mask and the actual Ni dot is only ~1%. In addition, the current density and capacitance per unit area were calculated using the area of dots from the actually measured diameter of Ni dots using the optical microscope for both the control and RTP samples. Figure 3 shows the leakage current density of the control oxynitride and that of the oxynitride subjected to RTP processing at 1100°C in helium containing trace oxygen (~300 to 600 ppm). The EOT, flatband voltage (V_FBL), and doping concentration can be obtained using experimental C-V curves and theoretical C-V curves simulated using Berkeley Quantum (QM) simulator (see Fig. 4). As shown in Fig. 3, the leakage current of the control oxynitride sample is ~1.0 × 10⁶ A/cm² at |V_FBL| = 1 V, which is comparable to that reported in the International Technology Roadmap for Semiconductors and by other researchers. Because the I-V curves of the control oxynitride from Freescale Semiconductor is very uniform from device to device, only one curve is shown here. After RTP at 1100°C in helium containing trace oxygen, the leakage current density is reduced by ~3.5 orders of magnitude or ~3000 times. Figure 3 shows 10 devices on the half-piece of the wafer that went through the RTP process. The I-V curves of the 10 devices are about the same with little variation. The I-V curves of both the control sample and the RTP samples exhibit a little kink at ~1.0 V. This kink only appears on p-type Si substrate. No kink was observed on n-type Si. Other researchers also observed a similar kink on I-V curves of MOS capacitors on p-Si substrates. To accurately determine the EOT, high-frequency (100 kHz) C-V measurements of the MOS capacitors with circular dimensions were carried out as shown in Fig. 4. The theoretical C-V curves obtained using the Berkeley QM simulator are also shown in Fig. 4. The EOT of the control
oxynitride is 16.2 Å, which is very close to its nominal value (15.5 Å). The EOT of the RTP sample is 18.2 Å. Thus, there is ~2 Å oxide regrowth. Slight oxide regrowth is a key factor for the observation of large leakage-current reduction. The EOT extracted from the experimental C-V curves using the Berkeley QM simulator is in agreement with that measured optically using a spectroscopic ellipsometer (J. A. Woolam M3000V). Usually, for every 2 Å increase in oxide thickness, there is about a one order of magnitude leakage current reduction. Therefore, after subtracting the effect of the 2 Å oxide regrowth, the net leakage-current reduction is ~2.5 orders of magnitude or ~300 times. Both I-V and C-V curves shown in Fig. 3 and 4 strongly suggest that the large leakage-current reduction of industrial SiON wafers with proper RTP is reliable and reproducible.

Conclusions

We have developed a bilayer resist lithographic method based on all-organic resist, developer, and resist remover to fabricate Ni-gate MOS capacitors to validate the reduction of gate leakage current in SiON wafers by PECE. Using this lithographic method, Ni-gate MOS capacitors based on industrial SiON wafers were fabricated. Experimental I-V and C-V curves, together with the C-V curves simulated using the Berkeley QM simulator, demonstrate that a large leakage-current reduction (~300×) can be reliably and reproducibly achieved on industrial SiON wafers after proper RTP.

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References