

Evidence of enhanced phonon-energy coupling in SiO₂/Si

Pangleen Ong and Zhi Chen^{a)}

Department of Electrical and Computer Engineering, University of Kentucky, Lexington, Kentucky 40506
and Center for Nanoscale Science and Engineering, University of Kentucky, Lexington, Kentucky 40506

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The authors designed special *pn* junctions to examine the recently discovered phonon-energy-coupling enhancement effect. They found that the breakdown voltage of the silicon substrate is increased by 0.3 V after rapid thermal process (RTP), whereas it remains the same for diodes annealed in furnace with the same parameters as those in RTP. The increase in breakdown voltage of silicon is caused neither by dopant redistribution nor increased contact resistance after RTP but due to its intrinsic properties, i.e., stronger Si–Si bonds. The strengthening of Si–Si bonds is caused by coupling of the phonon energy from silicon to thin oxide. © 2007 American Institute of Physics. [DOI: 10.1063/1.2714197]

The major obstacle for scaling metal-oxide-semiconductor (MOS) transistors is the exponential increase in gate leakage current as oxide/oxy-nitride is scaled down to below 3 nm.^{1–3} If the leakage current of the oxide/oxy-nitride can be reduced by three to four orders of magnitude through the structure modification, it may be further scaled down to the ultimate limit. Recently, we reported that the leakage current of ultrathin SiO₂ gate oxides is reduced by four to five orders of magnitude due to the phonon-energy-coupling enhancement (PECE) effect induced by rapid thermal process (RTP) and deuterium (D) anneals.^{4–6} In our previous publications, we showed that both Si–D and Si–O bonds are strengthened due to the PECE effect.^{4–7} The Si–D bonds are strengthened because hot-carrier degradation of MOS transistors is dramatically reduced after RTP and deuterium anneals.^{6,7} The increase in oxide breakdown voltage by 30%–40% suggests that Si–O bonds are also strengthened due to the PECE effect.^{4–6} An interesting question is raised: How about the Si–Si bonds? If there is evidence that the Si–Si bonds are strengthened due to the PECE effect, it will be more convincing that the PECE effect plays a major role in leakage current reduction.

We showed by using Fourier transform infrared spectroscopy that there is no PECE effect if the oxide is thick (80 nm) because it is hard to induce any microstructure change of oxide by thermal stress when it is too thick.⁶ Therefore, it is unlikely to induce any microstructure change of a silicon wafer because it is too thick (~300–500 μm). If the silicon wafer's breakdown voltage is increased after RTP and deuterium anneals, on which a thin oxide layer is covered, the only explanation to this is that the phonon energy of the Si–Si bonds is coupled to the thin oxide, as shown in Fig. 1. In this letter, we will show that the Si–Si bonds are indeed strengthened after RTP and deuterium anneals by measuring the breakdown voltage of specially designed *pn* junctions.

We designed special *pn* junction diodes as shown schematically in Fig. 2. On one side of the substrate is a layer of thermally grown oxide and on the other side are *pn* junction diodes. The device fabrication process started with the

growth of a thick thermal field oxide (5000 Å) on the *p*⁺ substrate ($\rho=3.8\times 10^{18}$ cm⁻³). After opening diffusion windows on the field oxide at the back side of the wafer using positive photoresist (Shipley S1183), spin-on phosphorus dopant source (Filmtronics P509) was coated on the wafer and cured at 150 °C for 10 min on a hot plate. Constant source diffusion was carried out at 1000 °C for 1 h at 10% O₂ and 90% N₂ and the *n*⁺ region ($n=1\times 10^{21}$ cm⁻³) ~0.5 μm deep was formed on the *p*⁺ substrate. After opening windows for the *p*⁺ substrate region and removal of the field oxide on the front side using buffered-oxide etch (BOE), a thin oxide of 150 Å was thermally grown on the wafer. The *pn* junction structure on the back side of the wafer was etched in BOE to remove the additional 150 Å oxide, while the thin oxide (150 Å) on the front side of the wafer was protected using hard-baked photoresist. RTP at 1050 °C in pure nitrogen was then carried out for 4 min. Ohmic contacts were formed by lithography using negative photoresist (Microchem SU-8), thermal evaporation of Al, and post-metal-annealing in D₂ at 450 °C for 30 min. In order to rule out any effect that may be caused by dopant redistribution in RTP, an identical sample that went through the same fabrication processes except that, instead of annealing using RTP, it was annealed in furnace at 1050 °C in

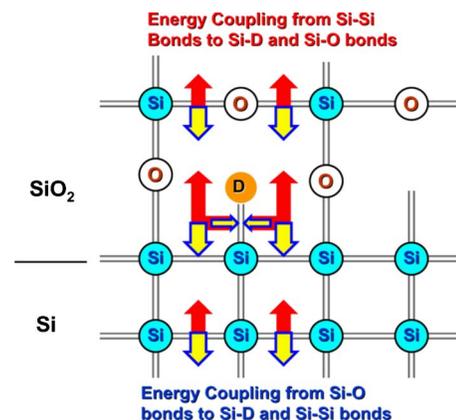


FIG. 1. (Color online) Schematic of phonon-energy coupling from Si–O bonds to Si–D and Si–Si bonds (open block arrows) and that from Si–Si bonds to Si–D and Si–O bonds (solid block arrows).

^{a)} Author to whom correspondence should be addressed; electronic mail: zhichen@engr.uky.edu

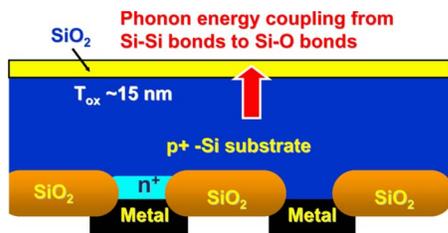


FIG. 2. (Color online) Schematic of a special pn junction diode with oxide of 15 nm on the other side of the substrate. The breakdown voltage of the diode was studied to show the strength of the Si-Si bonds of the substrate.

N_2 for 4 min (referred to as furnace anneal), was used for comparison.

Figure 3 shows I - V characteristics of a forward-biased pn junction diode. For $V < 0.7$ V, the current exhibits an exponential relationship with the forward-biased voltage. There is no difference between the control sample and the furnace-annealed as well as RTP-annealed samples in the exponential regime. For $V > 0.7$ V, the current of the RTP- and furnace-annealed samples increases slower than that of the control sample because of the large contact resistance induced by RTP and furnace anneals. In order to study the contact resistance issue in more detail, I - V curves on the linear scale for the forward bias are shown in the inset of Fig. 3. The diode can be modeled as an ideal diode with a series resistance which may be caused by dopant redistribution or nonideal contact after RTP and furnace anneals. The voltage applied across the diode can be expressed as $V \approx V_d + IR_s$, where V_d is the turn-on voltage of the ideal diode (~ 0.7 V) and R_s is the series resistance. The series resistance can be estimated from the I - V curves in the inset of Fig. 3. The series resistances of the control, RTP-, and furnace-annealed samples are ~ 10 , 40, and 75 Ω separately. It is the series resistance that causes the deviation of I - V curves away from the ideal exponential relationship. The impact of the series resistance on I - V curves is only effective at large current (> 1 mA). For current lower than 1 mA, the deviation is very small. This can be explained using the above simple diode model. The voltage deviation from the ideal diode can be expressed as $\Delta V = IR_s$. For $I = 1$ mA, ΔV is only 10 mV for the control sample, 40 mV for the RTP-annealed sample, and 75 mV for the furnace-annealed sample. Excluding the impact of the series resistance, it is clearly shown in Fig. 3 that the I - V curves for all samples in the forward-bias voltage are identical.

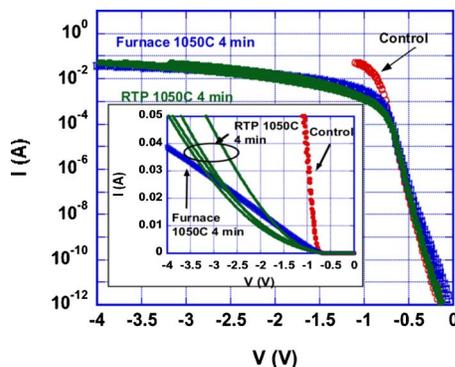


FIG. 3. (Color online) I - V characteristics of the forward-biased pn junction diode.

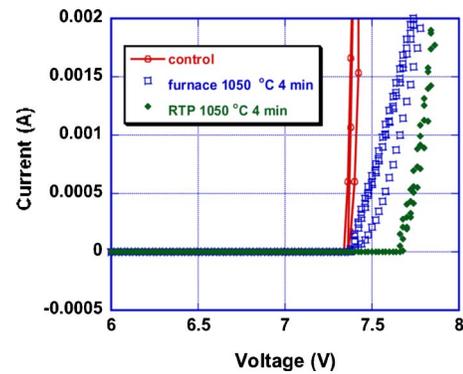


FIG. 4. (Color online) I - V characteristics of the reverse-biased pn junction diode.

It is more interesting to examine the breakdown voltage of the pn junction diode as shown in Fig. 4. It can be seen from Fig. 4 that the breakdown voltage of the Si substrate ($p = 3.8 \times 10^{18} \text{ cm}^{-3}$) is increased after RTP anneal. The breakdown voltage of the control sample is exactly the same as that of the furnace-annealed sample despite the large contact resistance of the furnace-annealed sample. Figure 5 shows the same I - V curves as those in Fig. 4 in log scale so that we can closely examine the breakdown phenomenon. It can be seen that the breakdown voltage is increased by 0.3 V after RTP. After breakdown, the current increases very sharply even on the log scale, suggesting that it is avalanche breakdown. From Figs. 4 and 5, it can be seen that the breakdown voltage is 7.4 V for the control and furnace-annealed samples, and 7.7 V for the RTP-annealed sample. According to Sze,⁸ for junctions with breakdown voltages in excess of $6E_g/q$, i.e., 6.6 V, the mechanism is avalanche multiplication. Therefore, the breakdown in our pn junctions is avalanche multiplication. Although the p -substrate doping is very high ($p = 3.8 \times 10^{18} \text{ cm}^{-3}$), it is still in the avalanche regime because the junction is not a real abrupt junction but something between the abrupt junction and a linear graded junction due to diffusion.⁸ Is the voltage increase really due to stronger Si-Si bonds or because of reduced dopant concentration or large contact resistance after RTP? In order to answer this question, we carried out sample anneal in furnace using the same parameters as those of RTP (1050 $^\circ\text{C}$ in N_2 for 4 min). From Figs. 4 and 5, it can be seen that there is no difference in breakdown voltages between the control sample and the furnace-annealed one. This may suggest that the dopant redistribution after thermal anneal is very small because

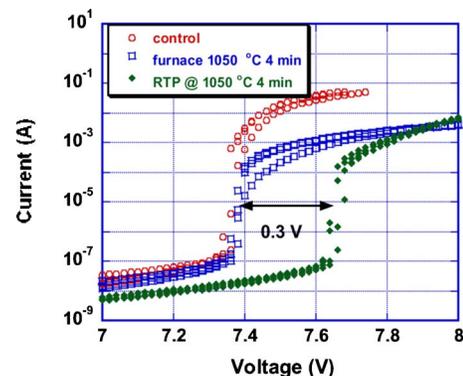


FIG. 5. (Color online) I - V characteristics of the reverse-biased pn junction diode.

the breakdown voltage is strongly dependent on the dopant concentration.⁸ Does the contact resistance affect the breakdown voltage? The voltage change due to the contact resistance is expressed as $\Delta V = IR_s$ and can be estimated using the R_s values obtained in the forward bias. As shown in Fig. 5, at breakdown, the current varies from 10^{-7} to 10^{-4} A, leading to $\Delta V = 1 \mu\text{V} - 1 \text{ mV}$ for the control sample, $4 \mu\text{V} - 4 \text{ mV}$ for the RTP-annealed sample, and $7.5 \mu\text{V} - 7.5 \text{ mV}$ for the furnace-annealed sample. All of them are much less than 0.3 V (300 mV) and thus are negligible. Therefore, the contact resistance does not play any role in breakdown voltage increase. The contact resistance plays a significant role only when the current is larger than 0.1 mA. Saturation of I - V curves on the log scale for $I > 0.1$ mA in Fig. 5 confirms the above suggestion. Therefore, neither the dopant redistribution nor the increase in contact resistance causes an increase in breakdown voltage. The sole reason for the increase in breakdown voltage of Si is due to its intrinsic properties, i.e., stronger Si-Si bonds after RTP.

We observed that there is no PECE effect when the oxide is too thick (80 nm).^{5,6} Therefore it is unlikely that RTP can

induce the structure change on the thick Si substrate (0.3 mm). Thus the strengthening of Si-Si bonds may be only caused by the thin oxide (15 nm) on the other side of the diode. This may suggest that phonon energy is coupled from the Si-Si bonds to Si-O bonds after RTP.

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